High Temperature Electronics Packaging

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Abstract

Materials and processes are being developed for packaging of low and medium power, high temperature electronics (up to 500°C). Ceramic (Al₂O₃ and AlN) hermetic packages are being used. Die attach techniques based on patterned Au bumps, Au-Si and off-eutectic Au-Sn have been demonstrated. Au thermosonic wire bonding provides a monometallic interconnect system between the die and the package pads. Both metallized ceramic and metal lids were vacuum solder sealed with off-eutectic Au-Sn. The sealing process had to be optimized to prevent growth of Ni-Sn-Au crystals during the liquidus phase of the sealing process. Assembly process details and initial characterization results are presented.

Introduction

Electronics and the ability to sense, compute, communicate and actuate have revolutionized the way mankind works, explores and relaxes. Consumer electronics with typical operating environments of 0°C to +85°C, is the largest electronics market segment. Military electronics with temperature ranges from -65°C to +125°C are less than 1% of the electronics market while automotive electronics with some under hood applications ranging from -55°C to +150°C are less than 5%. However, there are applications for electronics that operate at much higher temperatures. These include: space exploration (the surface of Venus is 485°C); oil and gas exploration and production (down hole temperatures to 325°C); and distributed controls for aircraft (150°C to 350°C). Thermal protection systems such as dewars and phase change materials may be used to protect conventional temperature range electronics operating in these environments for limited periods of time. For longer duration applications, complex thermal management systems such as fluid cooling are used to maintain the electronics at lower temperatures. In both cases, this adds significantly to the size, weight and cost of the system while introducing additional failure points. The ability to operate electronics at the ambient temperature will simplify the electronics system and enable the use of electronics in some applications where it is not possible today.

The availability of high temperature passives (resistors, capacitors and inductors) [1-4] and active devices (silicon-on-insulator, SiC, and GaN) [5-10] are opening opportunities to develop high temperature electronic systems. Just as conventional bulk Si devices are not suitable at 300°C, commercial plastic packaging is not suitable. The polymers and solders used in consumer and even military electronics decompose or melt at temperatures less than 300°C. The new lead-free solders: Sn-Ag (m.p. 221°C); Sn-Cu (m.p. 227°C); and Sn-Ag-Cu (m.p. 217°C) only provide a marginal increase in temperature over eutectic Sn-Pb (m.p. 183°C).

In this work, commercially available hermetic ceramic packages (Al₂O₃ and AlN) are being used. Additionally, direct bond copper (DBC) substrates have been used in some experiments. Several Au-based die attach technologies have been investigated at 325°C and 500°C. Thermosonic Au wire bonding was used for die-to-package electrical interconnections. Finally, metal and metallized ceramic lids were vacuum solder sealed to the package using off-eutectic Au-Sn. The ongoing packaging development is discussed in the following sections.

Die Attach

Au and Au alloy die attach materials are being investigated. The requirements for die attach are a function of the power dissipation of the device and the application. A die attach process for low
power die was developed based on thermocompression bonding with patterned Au die attach. The simplest pattern, made of individual bumps, would best answer applications requiring only lower die shear strength. Requirements of higher shear strengths would require more complex patterns. As a baseline, we evaluated the simplest configuration of bump patterns as illustrated in Figure 1. The Au bump pattern is thermosonically bonded to the base of the package using a conventional thermosonic wire bonder. The die is then positioned over the bump pattern and bonded using time, temperature and pressure as parameters. Alternately, the bump pattern could be plated onto the back of the SiC wafer prior to sawing.

Two methods were used for die attach: 1) static temperature/pressure using a vacuum furnace and 2) dynamic temperature/pressure using a thermocompression flip chip bonder. An SST vacuum furnace was used for the static assembly. A weight of 520 grams (for a pattern with 8 bumps) was applied to the die using a special collet designed to apply the bonding force to the perimeter of the die rather than the die face to prevent damage to the passivation, mesa structures, air bridges, etc. in the active die area. The thermal profile had a peak temperature of 550°C, held for 5 minutes. This is a batch process. For the dynamic bonding, a thermocompression flip chip bonder was used. This also included a specially designed collet to apply 2500 grams force for a pattern with 25 bumps. The thermal profile had a peak temperature of 400°C, held for 10 minutes. The bonding force required increased, corresponding to an increase in the number of bumps in the pattern. The die shear strength also increased, but not linearly, as the number of bumps increased. Thus a trade-off can be made between bonding force and die shear strength. An x-ray image of a die assembled into an AlN package using six Au bumps is shown in Figure 2.

To evaluate the thermal cycle performance of the Au patterned die attach, thermal cycle testing was performed on die assembled with the vacuum oven into a 16 lead Al₂O₃ SOIC package with a pattern of 8 Au bumps. The SiC die was 3.48mm x 3.48mm. The thermal cycle profile from +45°C to +325°C in air is shown in Figure 3. The die shear results are shown in Figure 4. There was an initial decrease in shear strength during the first 500 thermal cycles which then stabilized. The decrease in shear strength is believed to be due to annealing of the Au bump. Additional work is underway to optimize the bonding process and increase the initial shear strength.

Figure 1. Illustration of Au Pattern Die Attach.

Figure 2. X-ray Image of Die Attached Using a Pattern of Six Au Bumps.

Figure 3. Thermal Cycle Profile.
The patterned die attach should be capable of 500°C operation. To test this, die were assembled on to Ni/Au plated DBC Al₂O₃ substrates and stored at 500°C in air. In this case, patterns with 25 bumps were used per die. The shear test results are shown in Figure 5. At 500 hours, the failure mechanism was not failure of the die attach. With 500°C storage, the Au, Ni and Cu interdiffused and the Cu and Ni oxidized. During shear testing, layers of the oxidized substrate metallization scaled off. The die remained bonded to the oxidized metal layer. For hermetically sealed packages, oxidation of the package metallization within the cavity should not be an issue. A new test is underway to evaluate Pd/Au plated over refractory Mo-Mn. The Mo-Mn should not diffuse through the Pd and Au and while the Pd and Au will interdiffuse, Pd oxidation should not be an issue. It is expected this approach will also be suitable for non-hermetic, low power packaging.

Johnson, et. al. [11] have previously demonstrated off-eutectic Au-Sn die attach for high temperature SiC power transistor attachment. Thick Au (20µm) is plated onto either the backside of the die or the substrate. During die attach, the melting point of the Au-Sn increases as the wt% of Au in the die attach layer increases by dissolving Au from the die or substrate metallization. A new approach has been developed to achieve the off-eutectic
composition. Au foil 100µm thick is electroplated with 4µm of Sn on both surfaces. With this thickness ratio, the 108µm thick perform is 97wt.% Au. During the die attach process; the Sn layers liquify, rapidly dissolving Au. As the Au dissolves, the melting point of the liquid increases. Once the liquid layers solidify, solid state Sn diffusion continues during the high temperature soak in the die attach thermal profile. If equilibrium is achieved during the die attach process, the solidus point of the die attach would approach 700°C as shown by the dotted line (97wt.% Au) in the Au-Sn phase diagram (Figure 8).

Dissolution of additional Au from the die or substrate would further increase the solidus temperature. The key to the die attach process is to allow sufficient soak time at temperature for the Sn to diffuse to a low enough concentration throughout the die attach layer, so that the solidus temperature exceeds the maximum application temperature. The Sn will continue to diffuse toward the equilibrium concentration during the high temperature service life of the assembly. The final equilibrium Sn concentration is complicated if the Sn forms intermetallics with metallization layers on either the back of the SiC die or the substrate. In some cases, the equilibrium Sn concentration in the Au die attach layer can approach 0% as the Sn is consumed by intermetallic formation. It has been shown that in the case of off-eutectic Au-Sn die attach on DBC with electroplated Ni/electroplated Au on Cu, there is significant interdiffusion and intermetallic formation between the Au, Ni, Cu and Sn after 2000 hours at 400°C [11]. The die shear strength, however, remained high (>100kg-f for a 3.75 mm x 3.75 mm SiC die).

In the case of DBC with electroless Ni:P/electroless Au, the Ni:P layer is less reactive during 400°C storage. There is some Cu diffused into the Ni:P layer after storage at 400°C (Figure 9), but the Ni:P layer remains largely intact. The Ni:P layer acts as a diffusion barrier to the diffusion of Au and Sn into the Cu layer, but is not effective in preventing the diffusion of Cu into the Au-Sn layer. This differential diffusion results in Kirkendall void formation (Figure 9) at the Cu-to-Ni:P interface and a reduction in die shear strength (73kg-f) after 2000 hours. With Au-Sn die attach, electroless Ni:P is not recommended for high temperature applications. Since electroless plating is advantageous in some situations, experiments are currently underway on DBC with electroless Ni:B instead of electroless Ni:P.

With DBC, a series of intermetallics formed including Cu-Ni-Sn. Additional tests are underway to evaluate Ni/Au and Pd/Au plated on refractory Mo-Mn. In these constructions, Cu containing intermetallics will not be formed: Ni-Au-Sn and Pd-Au-Sn intermetallics are predicted. The effect of these intermetallics on die shear strength will be studied.

Figure 10 shows the cross section of a die attach stack for a SiC power device. A Ni-clad Mo tab is brazed to a DBC substrate with eutectic Cu-Ag
Figure 9. Cross Section of Off-eutectic Au-Sn Die Attach on DBC Substrate with Electroless Ni:P after 2000 hours at 400°C.

braze. The Mo tab will provide a near CTE match to the SiC die. The substrate is then electroplated with Ni/Au. The SiC die is attached to the plated Mo tab with the Sn/Au/Sn perform. In this configuration, the Mo tab separates the Sn from the Cu; thus Cu containing intermetallics will not form. The high temperature reliability of this construction is being evaluated.

Figure 10. Cross Section of SiC Power Die Assembly.

Wire Bonding

Small diameter Au and Pt wire bonding has been demonstrated with Au wire bonds on SiC and Au substrate metallization [12]. Au wire provides higher electrical conductivity, while Pt has higher mechanical strength. Large diameter Au wire has also been demonstrated for SiC power devices [11]. Au ribbon bonding is currently being evaluated for high current applications.

Hermetic Packages

For low and medium power applications, Al₂O₃ and AlN ceramic packages have been selected. Metal packages were considered, but the CTE of Kovar® varies significantly as a function of temperature. AlN (4.5ppm/°C) provides a near perfect match to SiC (4.2ppm/°C); however, open tooled AlN packages are limited. A wide variety of Al₂O₃ packages are commercially available, but the CTE of Al₂O₃ is 6.5ppm/°C. For the small SiC die currently available, the CTE mis-match to Al₂O₃ is not a significant issue, but as the available SiC die size increases this will be more of a concern. Both 16 lead Al₂O₃ SOIC and 8 I/O leadless AlN packages (Figure 2) have been used.

The lids provided with the Al₂O₃ SOIC package were Ni/Au plated Kovar with a pre-deposited Au-Sn perform. These are intended for conventional temperature range applications. By plating a thick Au layer on the package seal metallization, a high temperature package seal can be obtained as described in the Au-Sn die attach procedure. Needles were observed in the seal region with the initial sealing temperature profile, Figure 11. Cross sectional analysis, Figure 12, revealed the needles were Au-Ni-Sn. The Au-Sn reacted with the Ni layer during the sealing process to form an intermetallic. While the Au-Sn was liquid, intermetallic crystals grew through the liquid and extended beyond the liquid surface. Packages sealed with the initial temperature profile did pass gross and fine leak testing (1.6x10⁻⁹ atm cm² He/sec). Parts stored at 300°C for 1000 hours showed no further growth of the needles.

By modifying the lid seal process to limit the time in the liquid state, the needles were eliminated. A Au plated, Ni-clad Mo lid and a refractory metallized, Ni/Au plated AlN lid were used with the AlN package. An eutectic Au-Sn perform and thick Au plated on either the package or the lid provided a high temperature
seal, Figures 13 and 14. No needles were observed in the seal area.

Figure 11. Example of Needles in Au-Sn Lid Attach Using Initial Lid Seal Temperature Profile.

Figure 12. Cross Section of Lid Attach with Initial Lid Seal temperature Profile. W observed is refractory metallization of Al\(\text{2O}_3\) package.

Figure 13. Photograph of Sealed AlN Package.

Figure 14. Cross Section of Lid Seal with Au Plated, Ni-Clad Mo lid.

Conclusions

The availability of high temperature electronics will enable new systems for space exploration, oil and gas exploration/production and distributed controls for more electric aircraft, ships and ground vehicles. Packaging is a key element of this development. Ongoing research in die attach and package sealing have been described. In particular, patterned die attach, Au-Si and off-eutectic Au-Sn die attach have been discussed. These materials and processes are promising for low-to-medium power applications at 300°C (Au-Si) and up to 500°C (Au bump and Au-Sn). Off-eutectic Au-Sn package sealing has also been described. Alternate plating finishes (Ni:B and Pd) are currently under investigation.

References