Assembly with Chip Scale Packages

R. Wayne Johnson
Ginn Professor of Electrical & Computer Engineering
Laboratory for Electronics Assembly & Packaging (LEAP)
Auburn University
162 Broun Hall/ECE Dept.
Auburn, AL 36849-5201
334-844-1880 (ph.)
334-844-1898 (fax)
johnson@eng.auburn.edu

Chip Scale Packages

- Outline
  - Introduction
  - Chip Scale Packages
  - Assembly
  - Reliability
Chip Scale Packages

CSPs - Linear dimensions of package $ \leq 1.2x$ the dimensions of the die

Comparison

[Images of chip scale packages and comparison]
Technology Comparison

- **Advantages of CSPs**
  - Speed of Testing for Known Good Die (KGD)
  - Handling
  - Assembly
  - Rework
  - Die Protection
  - Ability to Adjust to “Die Shrink or Expand”
  - Standards
  - Infrastructure
  - Reliability without Underfill

- **Advantages of Flip Chip**
  - Size
  - Cost
  - Weight
  - Thermal Performance
  - Electrical Performance

CSP Types

- **Rigid Interposer**
  - Typically a Ball Grid Array Type Package with Higher Density, Smaller Solder Ball Diameter, Smaller Solder Ball Pitch, Thinner but Fairly Stiff Interposer Board.

- **Flex Interposer**
  - Typically a Ball Grid Array Type Package with Higher Density, Smaller Solder Ball Diameter, Smaller Solder Ball Pitch, Thinner and Flexible Interposer Board.
CSP Types

- **Lead Frame Interposer**
  - Typically Similar to a Plastic Encapsulated Package but with a Leadframe that Extends Over the Chip

- **Wafer Level Assembly / Wafer Scale**
  - Various Technologies (Most Look Like Flip Chips with large solder balls) Where the Packaging is Performed on the Chips in Wafer Form

CSP PACKAGES

Example - Rigid Interposer

FBGA - Fine Pitch BGA
CSP PACKAGES
Example - Flex Interposer

μBGA

CSP PACKAGES
Example - Lead Frame Interposer
CSP PACKAGES
Example - Wafer Scale Processing

63Sn/Pb Solder Bump
Not to Scale

Typically a Ball Grid Array Type Package but with Higher Density,
Smaller Solder Ball Diameter, Smaller Solder Ball Pitch, Thinner
but Fairly Stiff Interposer Board (Ceramic or Laminate).

“Rigid” Interposer
CSP PACKAGES

“Rigid” Interposer

Xilinx CSP’s
CSP PACKAGES
“Rigid” Interposer

Amkor ChipArray CSP

CSP PACKAGES
“Rigid” Interposer
CSP PACKAGES
“Rigid” Interposer

Pentium PC on a Card - Intel CSP’s

![Image of Pentium PC on a Card - Intel CSP’s]

CSP PACKAGES
“Rigid” Interposer

Pentium PC on a Card - Intel CSP’s

![Diagram of Stud Bump CSP structure]

Intel Pentium Die
- Die size: 9.17 x 9.93 mm
- Pads per Die: 359
- Minimum pad pitch: 85 μm

CSP characteristics
- CSP size: 13 x 1.01
- Lands per CSP mm
- Land: 0.6mm / 0.8mm pitch
- Land Over Coat Opening: 0.4mm
- Number of Layers
- Line Space: 2565 μ
- Substrate Material
- 96% Alumina

UNIT: mm
CSP PACKAGES
“Rigid” Interposer

Pentium PC on a Card - Intel CSP’s

Motorola SLICC
“Slightly Larger Than IC Carrier”

CSP characteristics
CSP size: 15 x 2mm max.
Lands per CSP: 334
Land: 0.6mm / 0.8mm pitch
Land Over Coat: Opening 0.4mm
Number of Layers: 2
Line / Space: 25/45 μm
Substrate Material: 99% Alumina

MT2C Die
Intel
Die size: 6.47 x 6.50mm
Packs per Die: 340
Minimum pad pitch

Organic Substrate
High Lead Solder Balls
Underfill
Eutectic Solder Balls
Next-level Board
CSP PACKAGES

“Rigid” Interposer

Motorola SLICC
“Slightly Larger Than IC Carrier”

CSP PACKAGES

“Rigid” Interposer

Motorola SLICC
“Slightly Larger Than IC Carrier”
CSP PACKAGES
“Rigid” Interposer

IBM - Ceramic Mini-BGA

- Thermal Paste
- Chip
- Decoupling Capacitor
- Ceramic Substrate
- C4 Solder Balls
- Cap
- Mini-Ball Grid Array
  0.25mm balls on 0.5mm pitch

JEDEC MO-195 FBGA* - Standard CSP

* Fine-Pitch BGA
  - Uniform Square Outline
  - 0.50 mm Contact Pitch
  - 0.30 mm Ball Diameter
  - 4 - 21 mm Size Range
  - Thin (1.20 mm) Profile
  - 36 to 1681 I/O
CSP PACKAGES
“Rigid” Interposer

CSP Standards under Consideration (i.e. Typical Products)

- **Array Pitch**
  0.40, 0.50, 0.65, 0.75, and 0.80 mm

- **Contact Diameter**
  0.20, 0.25, 0.30, 0.35 and 0.40 mm

- **Package Thickness**
  L = Low, T = Thin, V = Very Thin, U = Ultra-thin

- **Package Size**
  L and W Separately Controlled

- **Tolerancing**
  Contact Location and Coplanarity

- **Primary Datum**
  Referenced to Body or Array Contact Features

“Unofficial” CSP Terminology - Profile Height Variations

- **(L) Low Profile** 1.21 mm to 1.70 mm
- **(T) Thin Profile** 1.01 mm to 1.20 mm
- **(V) Very Thin Profile** 0.81 mm to 1.00 mm
- **(W) Very-Very Thin** 0.66 mm to 0.80 mm
- **(U) Ultra-Thin Profile** 0.65 mm maximum
CSP PACKAGES

“Rigid” Interposer

FBGA 112  
Rohm

FBGA 128

FBGA 180

FBGA 192

Stacked etCSP™

Courtesy: Amkor Technology
Stacked etCSP™
Isometric Side View

Courtesy: Amkor Technology

Package Stacking
Stacked CSP Structure (Rigid)

- Die Attach Film (or Paste)
- Die Attach Paste
- Solderball: 63 Sn/37 Pb, 0.4 mm Diameter, 0.8 mm Ball Pitch
- Dielectric: Semi-rigid 2-layer laminate (shown)
- Soldermask
- Gold Wire

Note: Via Capture Pad will be offset from SB Land – not as shown

Courtesy: Amkor Technology
Four Die Stack: Different size die

Courtesy: Amkor Technology

Four Die Stack: Same size die

Courtesy: Amkor Technology
Stacked Packages/Die

CSP PACKAGES
Flex Interposer

FBGA - Fine Pitch BGA
CSP PACKAGES
Flex Interposer

Texas Instruments Micro Star BGA

Micro Star Cross-section
CSP PACKAGES
Flex Interposer

fleXBGA and TapeArray BGA

Courtesy: Amkor Technology
**CSP PACKAGES**

*Flex Interposer*

**Tessera FµBGA™**

- Elastomer Overmold
- Die Face Up
- Elastomer layer

Wire Bond on Polyimide Flex Film

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**CSP PACKAGES**

*Flex Interposer*

**Tessera FµBGA™**

- 16.5 x 16.5mm, 608 I/O, 0.50mm Basic Pitch
CSP PACKAGES
Flex Interposer

Nitto-Denko Resin Molded CSP

Chip
Thermo-compression Bond
Inner Connection
Au or Au Plated Cu Bumps
Thermo-adhesive Polyimide
Tape Carrier
Polyimide

Solder Ball

Stacked CSP Structure (Tape)

Gold Wire
Mold Compound
Die Attach Film (or Paste)
Die Attach Paste
Dielectric
Non-reinforced 1-layer Polyimide dielectric (shown)

Solderball
- 63 Sn/37 Pb
- 0.45 mm Diameter
- 0.8 mm Ball Pitch

1.20 mm (max.)
0.75 mm
0.3 mm (min.)

Courtesy: Amkor Technology
CSP PACKAGES
Flex Interposer

Tessera μBGA

Optimized Encapsulant
Low Modulus Nubbin
CSP PACKAGES
Flex Interposer

Tessera μBGA
External Lead Configuration

Internal Lead Configuration

μBGA® X-Section
CSP PACKAGES
Flex Interposer

Tessera μBGA - Manufacturing Process

Final Product

CSP PACKAGES
Flex Interposer

Tessera μBGA
CSP PACKAGES
Flex Interposer

μBGA Attachment

cross section courtesy of Xetel

μBGA Examples

CSP PACKAGES
Flex Interposer

μBGA Examples
CSP PACKAGES
Flex Interposer

μBGA Examples

CSP PACKAGES
Lead Frame Interposer

Concept of a Lead on Chip (LOC) CSP

Typically Similar to a Plastic Encapsulated Package but with a Leadframe that Extends Over the Chip
CSP PACKAGES
Lead Frame Interposer

Fujitsu - CSP Evolution

(A) MF-LOC (Fujitsu)

(B) Tape-LOC

TI Japan Memory CSP

Solder Ball
Mold Compound
Gold Wire
Lead Frame
CSP PACKAGES
Lead Frame Interposer

Hitachi CSP

Fujitsu Bump Chip Carrier (BCC)

Meets JEDEC MO-185 Standard Outline
50% Height Reduction Vs SSOP
65% Area Reduction Vs SSOP
CSP PACKAGES
Lead Frame Interposer

Fujitsu’s Bump Chip Carrier (BCC)

A. Resist Formation
B. Etching

c. Plating
d. Resist Removal

CSP PACKAGES
Lead Frame Interposer

Fujitsu’s Bump Chip Carrier (BCC)

a. Die attach
b. Wire bonding
c. Molding
d. Terminal forming (Etching)
CSP PACKAGES
Lead Frame Interposer

**Fujitsu Bump Chip Carrier (BCC)**

*Image of Fujitsu Bump Chip Carrier (BCC)*

**BCC™ Leadless**
- Au Wire
- Die
- Resin
- Au Stud Bump
- Base (Insulator)

Terminal Structure:
- Resin protrusion
- 4 layer metal structure
- Ensuring wire bonding
- Preventing diffusion
- Ensuring solderability
- Ensuring durability

**LG Semicon Bottom Leaded Plastic (S-BLP) Package**

*Image of LG Semicon Bottom Leaded Plastic (S-BLP) Package*

- Gold Wire
- Molding Compound
- Adhesive
- IC
- Leadframe
- Bottom Pad Solder Plated
CSP PACKAGES
Lead Frame Interposer

LG Semicon Bottom Leaded Plastic (C-BLP) Package

Gold Wire
Molding Compound

Adhesive
IC

Leadframe
Bottom Pad Solder Plated

CSP PACKAGES
Lead Frame Interposer

LG Semicon Bottom Leaded Plastic (BLP) Package

<table>
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<th></th>
<th>SOJ</th>
<th>BLP</th>
<th>TSOP</th>
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<tbody>
<tr>
<td>Projected Area (mm²)</td>
<td>146.0</td>
<td>107.0</td>
<td>159.9</td>
</tr>
<tr>
<td>Volume (mm³)</td>
<td>3.76</td>
<td>0.85</td>
<td>1.25</td>
</tr>
<tr>
<td>Package Weight (g)</td>
<td>0.82</td>
<td>0.20</td>
<td>0.30</td>
</tr>
</tbody>
</table>
QFN

CSP PACKAGES
Wafer Level Assembly

Mitsubishi
*Chip Scale Package* (CSP)

Original Use of the Terminology CSP
CSP PACKAGES
Wafer Level Assembly

Mitsubishi Chip Scale Package (CSP)

[Diagram of Mitsubishi Chip Scale Package (CSP)]

CSP PACKAGES
Wafer Level Assembly

Mitsubishi Chip Scale Package (CSP)

[Diagram of Mitsubishi Chip Scale Package (CSP)]
CSP PACKAGES
Wafer Level Assembly

Mitsubishi Mold CSP
2nd Generation

- External Electrode Bump
- Transferred Copper Land
- Resin
- Inner Solder Bump
- LSI Chip
- Passivation Film
- Electrode Pad
- UBM
- Polyimide Film
- Wiring Conductor Pattern

CSP PACKAGES
Wafer Level Assembly

Mitsubishi Mold CSP

- 96 pin
- 256 pin
- 1024 pin
CSP PACKAGES
Wafer Level Assembly

Wafer Level W.A.V.E. Package

Copper circuit layers
Flexible link
Cu or Al circuitry on chip

Tessera - WAVE™ (Wide Area Vertical Expansion)

CSP PACKAGES
Wafer Level Assembly

Attach Wafer to Pellicle

Transient Liquid Phase Joining
CSP PACKAGES
Wafer Level Assembly

Inject Encapsulant

- Encapsulant Reservoir
- Vent
- Curved leads allow for lift

CSP PACKAGES
Wafer Level Assembly

Mass Placement of Solder Balls

- 300mm diameter spheres
CSP PACKAGES
Wafer Level Assembly

3D Xray Image of the Flexible Copper® Link

Ball Attach Pad
Die Bond Site
Flexible Copper Link

CSP PACKAGES
Wafer Level Assembly: FormFactor MOST

MOST Technology Processed Wafer
Au wire over-coated with Spring Alloy and Au

Redistribution Trace
Al Bond Pad
Adhesion Layer

Si Wafer

MicroSpring Contacts Structure Cross Section

Courtesy: FormFactor
CSP PACKAGES
Wafer Level Assembly: FormFactor MOST

MicroSpring Contacts
On a DRAM Die

Courtesy: FormFactor
## CSP PACKAGES
**Wafer Level Assembly**

### Flip Chip Technologies - Ultra CSP

<table>
<thead>
<tr>
<th>Package</th>
<th>Ball Pitch (mm)</th>
<th>PCB Pad Diameter (mm)</th>
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</thead>
<tbody>
<tr>
<td>UltraCSP 50</td>
<td>.50</td>
<td>.275</td>
</tr>
<tr>
<td>UltraCSP 65</td>
<td>.65</td>
<td>.300</td>
</tr>
<tr>
<td>UltraCSP 75</td>
<td>.75</td>
<td>.350</td>
</tr>
<tr>
<td>UltraCSP 80</td>
<td>.80</td>
<td>.350</td>
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</table>

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## CSP PACKAGES
**Wafer Level Assembly**

### Flip Chip Technologies
**Ultra CSP**

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CSP PACKAGES
Wafer Level Assembly

Flip Chip Technologies - Ultra CSP

BCB1 Layer after Expose & Develop

Al/NiV/Cu UBM/RDL after Etch

CSP PACKAGES
Wafer Level Assembly

Flip Chip Technologies
Ultra CSP

BCB2 Layer after Expose & Develop
BCB1 Layer

63Sn/Pb Solder Bump
Not to Scale
CSP PACKAGES
Wafer Level Assembly

Flip Chip Technologies - Ultra CSP

Pitch 0.75 mm

0.54 mm

0.38 mm

0.61 mm

Die Size: 6.0 mm x 8.0 mm x
CSP PACKAGES
Wafer Level Assembly

Sandia miniBGA

CSP PACKAGES
Wafer Level Assembly

Sandia miniBGA

- Solder Bump
- Metal Layer #1
- Metal Layer #2
- Polyimide Layer #2
- Polyimide Layer #1
- Existing Passivation
- Existing Wire Bond Pad
CSP PACKAGES
Wafer Level Assembly

Sandia miniBGA

Substrates

Assembly
Solder Pads

- Two types of Land Pads
  - Non-Solder Mask Defined = Copper Defined Land Pad
  - Solder Mask Defined Land Pad
- The main difference between the land pad types is the size of trace/spaces and vias that can be used for escape routing of the signals and the shape of the solder balls after solder reflow (reliability).

Solder Mask Defined vs. Non-Solder Mask Defined
**Solder Mask Defined vs. Non-Solder Mask Defined**

- **Solder masked defined**
  - Increases Cu pad adhesion to substrate
  - For a given solder pad, the stand-off is higher (increases reliability)
  - Stress concentration points for crack initiation at solder mask/solder interface (decreases reliability)
Solder Mask Defined vs. Non-Solder Mask Defined

- Non-solder mask defined
  - Lower effective Cu pad adhesion
  - Lower stand-off height for a constant pad size
  - Often design smaller pads to increase stand-off height

Escape Routing

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<th>0.80 mm</th>
<th>0.75 mm</th>
<th>0.65 mm</th>
<th>0.50 mm</th>
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<tbody>
<tr>
<td>(6 mil)</td>
<td>(6 mil)</td>
<td>(5 mil)</td>
<td>(3 mil)</td>
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</table>

<table>
<thead>
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<th>e =</th>
<th>0.25 mm dia.</th>
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<tbody>
<tr>
<td>(6 mil)</td>
<td></td>
</tr>
<tr>
<td>(3 mil)</td>
<td></td>
</tr>
</tbody>
</table>
High Density Interconnect (HDI)

- Non-reinforced dielectric layers
  - Liquid or dry film
    - Photoimaged vias
    - Laser drilled vias
    - Plasma etched vias
- Reinforced dielectric layers
  - Laminate
    - Laser drilled vias

HDI Example
Pad-in-Via and Dogbones

Via-in-Pad
Printed Circuit Board (PCB) - Finish

- Fine pitch devices require a very uniform and flat surface finish as a means of controlling the uniform volume of solder paste at the attachment site.

- Common PCB Finishes
  - Hot Air (Sn/Pb) Solder Leveled (HASL)
  - Ni/Au electroless process
  - Ni/Au electroplating process
  - Pd/Ni or Pd/Cu electroless coating
  - Ag
  - Benzotriazole (BTA) Organic Solderability Preservative (OSP)

Hot Air Leveled Process (HASL)

- Solder dip and hot air solder leveling is a common PCB surface finish for solder attachment.
  - Sn/Pb coating is applied after the solder mask application, coating only the contact areas, plated holes and contact pads
  - Coated boards are cleaned, fluxed and dipped into molten solder.
  - While the alloy is still in the liquid state, excess material is blown off the contact surface with hot air, leaving a solder coated surface finish.
Issues related to HASL

- Uneven surface plating
- Crowning of solder on fine pitch and CSP sites
- Solder paste uniformity
- Tin/Copper intermetallic migration
- Extreme Thermal shock
  - Board warp
  - Delamination
  - Damage to the plated holes
  - Defects that may effect long term reliability.

Ni/Au Electroless Process

- Electroless Ni is applied over the exposed bare copper after solder mask coating process.
  - The fabricator will typically use the Sn/Pb plated circuit pattern as an etch resist and strip the Sn/Pb after etching.
  - Exposed attachment sites and holes are plated with the Ni using electroless plating process followed by a layer of gold by immersion process as well.
- Typical
  - Electroless Ni thickness : 125 - 200 µ in
  - Immersion Gold thickness : 3 - 8 µ in
Ni/Au Electroplating Process

- Electroplated Ni/Au is applied after hole plating.
- Ni/Au is resistant to the acid used to etch away copper.
  - This replaces the plating and subsequent stripping of Sn/Pb.
- This method can furnish finer lines and spaces.
- Typical
  - Electroplated Ni thickness : 100 - 150 µ in
  - Electroplated AU thickness : 3 - 5 µ in

A word of caution...

- The gold plating volume within the solder joint should be less than 3% and preferably less than 1% to avoid embrittlement of the joint and intermetallic formation.
  - Gold thickness will depend on solder volume
- Current industry issue with Electroless Ni/Immersion Au.
  - Low occurrence rate of failures in mechanical shock related to the immersion gold process
**Immersion Ag**

- Provides a solderable coating
- Ag dissolves into molten solder
- Growing in popularity

**Alternatives to Alloy Plating**

- As an alternative to plating, many companies have had success and economic advantage as well as a flat attachment surface with organic preservatives or pre-flux coatings over bare copper.
- As a means of retarding oxide growth on the bare copper attachment sites and via/test pads, a preservative or inhibitor coating is applied to the board. Organic/Nitrogen coatings such as, Benzotriazole or Imidazole are used instead of alloy finishes.
Advantages of OSP

- Multiple exposure capability
- Ease of visual inspection of deteriorated copper (if any)
- Excellent pad coplanarity
- Consistent solderability

Concerns of Coated boards

- Degrades in high humidity/temperature
- Limited (6-12 months) shelf life
- Physical contact can degrade coating
- Exposed copper will (in time) tarnish
Trade-offs in Surface Finish Selection

- No matter what, flat topography is a must
- HASL solder coating is not uniform.
- Ni/Au plating is uniform. May be the best as long as the thickness of Au is < 5 µ in, but expensive.
- Plating is more costly than coating.
- Coatings have limited shelf life

SMT Assembly Process Flow

1. Solder Printing
2. Print Inspection
3. Device Placement
4. Inspection
5. Reflow Solder Process
6. Clean and Inspection
7. Assembly Test
8. Package and Ship
Stencil Selection

- Stencil thicknesses, as well as the etched pattern geometry, determine the precise volume of solder paste deposited onto the device land pattern.
- Stencil alignment accuracy and consistent solder volume transfer is critical for uniform reflow solder processing.

Various types of Stencils

- Etched Stencils
- Laser Cut Stencils
  - Electropolished
  - Ni plated
- Ni formed Stencils
Chem Etch

As-etched    Electropolished

Etched Stencils

- Thickness ± 0.012mm
- Aperture Width
  ±0.05mm to supplied data
- Minimum Apertures
  - 0.15mm in 0.15mm thickness
  - 0.2mm in 0.2mm thickness
  - 0.25mm in 0.25mm thickness
Laser Cut Aperture

- Thickness $\pm 0.012\text{mm}$ of specified requirement
- Aperture Width better than $\pm 0.008\text{mm}$ to supplied data
- Minimum aperture $0.05\text{mm}$
- Positional Accuracy $\pm 0.013\text{mm}$ over $500\text{mm}$
Ni Electroformed

- Thickness ± 0.012mm of specified requirement
- Aperture Width ± 0.012mm to supplied data
- Minimum Apertures
  - 0.050mm in 0.1mm thickness
  - 0.075mm in 0.127mm thickness
  - 0.10mm in 0.150mm thickness
  - 0.127mm in 0.2mm thickness

Ni Formed Stencils
Materials Used for Stencils

- Stainless Steel (300 series)
  - more durable
- Nickel
- Brass
- Typical Thickness range of the Stencils
  - 0.1mm to 0.203mm

Solder Stencil

Top View
- Round apertures
- Square apertures

Side View
- Stencil apertures should be tapered to produce more uniform release of solder paste.
Stencil Geometry

- Optimum aperture shape in the stencil is TRAPEZOIDAL for fine pitch components
  - ensures good paste release and consistent volume
- In CSP packages, stencil opening can be greater than or equal to the diameter of the land pattern.

Chip-Scale BGA
Stencil Fabrication

1.3 - 1.5 mm (5 - 6 mil) Thick Solder Paste Stencil
Trapezoidal Aperture Recommended
Stencil Geometry (cont’d)

- Square openings have proven to be beneficial for BGA and CSP applications
- Square patterns have the following advantages
  - increase solder volume slightly
  - releases the paste from the stencil more uniformly than circular openings

Stencil Design

Area Ratio = \frac{\text{Area of Aperture Opening}}{\text{Area of Aperture Wall}}

Area Ratio > 0.66
**Recommended Solder Stencil Aperture**

for

**0.50 - 0.75 mm Pitch CSP Attachment**

For chemically etched stencil, corner radius is typically 1x stencil thickness.

---

**Impact of Solder Stencil Aperture Size**

Size-on-Size Aperture

Size-on-Size Solder Paste Print Pattern

Expanded Aperture

Over Print Solder Paste Pattern

0.25 0.30 mm Attachment Site
Solder Paste Print Profile

- CSP Land Pattern
- Solder Paste
- Solder Mask
- Over-Printed Solder Paste
- May Cause Increase in Solder Balls
- PC Board

Solder Paste

- Quality of the paste print is an important factor in producing high yield assemblies
- Paste is the vehicle providing
  - solder alloy that forms the final joint
  - flux necessary to clean the surfaces and promote wetting
  - hold components in place until the solder is reflowed
- Choice of solder paste determines thermal profile and reflow parameters
- Manufacturer’s suggested thermal profile should be referenced prior to manufacturing
Solder Paste (cont’d)

- Solder is a near eutectic alloy of 63Sn/37Pb
- Most fluxes are rosin based and classified as
  - R (nonactivated)
  - RMA (rosin mildly activated)
  - No clean
    - Flux residue is inert does not require cleaning
  - Water soluble organic acid (OA)

Paste Types

<table>
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<tr>
<th>Type</th>
<th>None Larger Than (um)</th>
<th>Less Than 1% Larger Than (um)</th>
<th>80% Minimum Between (um)</th>
<th>10% Maximum Less Than (um)</th>
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<tr>
<td>1</td>
<td>160</td>
<td>150</td>
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<td>6</td>
<td>20</td>
<td>15</td>
<td>15-5</td>
<td>5</td>
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</table>
Comparison of Apertures to Solder Particles

Alternative Solid (non-collapsing) Contact

- **Solid Core Alloy**
  - Copper
  - Bronze
  - Nickel
- **Contact Finish**
  - 90Sn/10Pb
  - 63Sn/37Pb
  - Au over Ni
  - Au/Pd-Ni
- **Uniform Standoff height can be achieved**
- **Desoldering is practical**
- **Self centering reaction is reduced due to the lower solder paste volume**
- **To maximize self centering, solder contaminates and oxidation must be eliminated**
**Solid Copper Core Ball Contact**

- Solid Copper Core Ball Contact
- Solid Core Solder Coated Ball
- Polyimide Film
- Low Modulus Elastomer
- IC Die
- Encapsulation
- Bond Ribbon
- Coverlay Material

**SMT Assembly Process Flow**

1. Solder Printing
2. Print Inspection
3. Device Placement
4. Inspection
5. Reflow Solder Process
6. Clean and Inspection
7. Assembly Test
8. Package and Ship
Print Inspection

- Inspection of solder paste quality and uniformity control before attaching CSP is beneficial
- Solder rework is not practical and removal of the device is the only option
- Inspection, at this stage, includes measurement of both thickness and uniform coverage

SMT Assembly Process Flow

1. Solder Printing
2. Print Inspection
3. Device Placement
4. Inspection
5. Reflow Solder Process
6. Clean and Inspection
7. Assembly Test
8. Package and Ship
Word of Caution before Assembly

- Many types of CSPs are moisture sensitive.
- Store parts properly in dry environment.
- Do not open dry bags until ready to assembly.
- Dehydrate parts as necessary based on exposure and JEDEC moisture level.

JEDEC Moisture Sensitivity

<table>
<thead>
<tr>
<th>Level</th>
<th>Floor Life</th>
<th>Soak</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Conditions</td>
<td>Time</td>
</tr>
<tr>
<td>1</td>
<td>&lt;30°C 85%RH</td>
<td>Unlimited</td>
</tr>
<tr>
<td>2</td>
<td>&lt;30°C 60%RH</td>
<td>1 year</td>
</tr>
<tr>
<td>2a</td>
<td>&lt;30°C 60%RH</td>
<td>4 weeks</td>
</tr>
<tr>
<td>3</td>
<td>&lt;30°C 60%RH</td>
<td>168hrs</td>
</tr>
</tbody>
</table>

Joint IPC/JEDEC Standard J-STD-020A
JEDEC Moisture Sensitivity

- Following soak, parts are subjected to 3 reflow cycles
- Inspected:
  - Electrical
  - Visual for cracks
  - Acoustic microscopy for delamination

Placement and Alignment

- Pick and Place accuracy governs the package placement and rotational alignment
- Slightly misaligned parts (less than 50% off the pad center) will automatically self align during reflow
- Grossly misaligned packages (greater than 50% off pad center) should be removed prior to reflow as they can develop electrical shorts, leads to solder bridges, when subjected to reflow.
Methods for Package Placement

- Package Silhouette
  - Vision system locates the package outline
    - faster
    - ±0.1 mm accuracy

- Ball recognition
  - Directly locate on the solder ball array pattern
    - More accurate, but slow, because it requires complex vision processing

Vision System

Figure 1: Effect of placement equipment vision system on inspection of bump array packages; largerPackages typically placed via front lighting with bump array inspection. Back lighting was added to improve yield by reducing package reflection.
Lighting System

Figure 1. An on-axis illumination system used by some placement systems. FoCPS, a problem occurs when the system cannot recognize the component details. It relies upon accuracy.

Figure 2. Off-axis, or "low-angle," illumination. Light rays reflecting off the CPs’ solder bumps enter directly into the lens, while those hitting the back/side go off at an angle, thus presenting good contrast for machine placement.

SMT Assembly Process Flow

1. Solder Printing
2. Print Inspection
3. Device Placement
4. Inspection
5. Reflow Solder Process
6. Clean and Inspection
7. Assembly Test
8. Package and Ship
Reflow

- Different Options
  - Infrared
  - Forced Air/Gas (Nitrogen) Convection
  - Mixed IR/Convection
  - Vapor Phase Soldering

Package Self Alignment at Reflow

How surface tension promotes self-centering placement of solder-bumped components during reflow begins with an example of a solder interconnect placed 50 percent on the pad (a). When the temperature reaches the flux-activation point, the paste forms a dome (b). Surfaces begin to wet and a solder meniscus forms during the liquidus stage (c). After which, sphere and plate join to form a solder column (d). Surface tension exerts a pull on the pad surfaces that helps to align the movement to relieve (e) toward equilibrium (f), a balanced condition between the top and bottom of the joint, whenupon movement stops to form the solder joint's final shape (g).
Oven Profile for Reflow Solder Process

SMT Assembly Process Flow
Clean and Inspection

- PCB cleaning depends on the flux used.
- X-ray radiograph techniques are used to inspect the solder ball reflow and the solder joint integrity.

SMT Assembly Process Flow

1. Solder Printing
2. Print Inspection
3. Device Placement
4. Assembly Test
5. Package and Ship
6. Reflow Solder Process
7. Clean and Inspection
8. Inspection

Flowchart showing the steps involved in the SMT assembly process.
Assembly test

- Test includes functional, burn-in, in-circuit as well as post assembly programming.

SMT Assembly Process Flow

- Solder Printing
- Print Inspection
- Device Placement
- Inspection
- Reflow Solder Process
- Clean and Inspection
- Assembly Test
- Package and Ship
CSP Underfill

- Initial data generated by thermal cycling
  - Demonstrated required reliability without underfill
  - Portable electronics also subjected to:
    - mechanical shock (dropping)
    - flexing (thin boards)
      - in assembly
      - keypads

➤ Underfill is needed in many portable products for mechanical shock & bending

Test Vehicle

- Four-layer test board
  - 10 CSP attachment sites per side.
  - Board was 2.95" by 7.24" by 0.042" thick.
  - The pads were 0.010” in diameter, non-solder mask defined with an electroless nickel/immersion gold finish
  - During the testing, no evidence of failure associated with ‘black pad’ was observed
Test Vehicle

- The CSP
  - 8mm
  - 0.5mm pitch, 132 I/O
  - TapeArray from Amkor Technology.
  - 14 x 14 array with only the outer three rows populated.
  - CSP was a daisy chain test part for continuity measurements
  - Silicon die was 3.98mm x 3.98mm

Underfill Issues

- Process:
  - Dispense
  - Cure
  - Rework
Underfill Options

- **Capillary Flow**
  - Non-reworkable (Underfill A)
    - Cure: 5 minutes @165°C conveyor oven
  - Reworkable (Underfill B)
    - Cure: 15 minutes at 150°C box oven
    - Designed to breakdown when heated to solder reflow (rework) temperature
- **Fluxing Underfill (Undefill C)**
  - Cures during reflow

Capillary Underfill Process 1

1. Print Solder Paste
2. Pick CSP
3. Place CSP
4. Dispense Underfill
5. Cure Underfill
6. Reflow
7. Clean (optional)
Capillary Underfill Process 1

- 4mil thick electropolished, Ni plated, laser cut stencil.
  - The aperture in the stencil was 0.010”
- Multicore CR-36 Type 4 solder paste
- MPM AP25 stencil printer
- Visual inspection
- Siemens F5 placement system
- Heller 1800 reflow oven
- Phoenix X-ray
- Camalot 3700 dispense system

Capillary Underfill Process 1

- Time delay between reflow and underfill
Capillary Underfill Process 1

- PWBs were dehydrated for 4-6 hours at 125°C

Capillary Underfill Process 1

- Flux residue effect
Cleaning

Aqueous clean using a 10% HYDREX DX solution in deionized water at 65-70°C

Capillary Underfill Process 2

- Pick CSP
- Flux
- Place CSP
- Reflow
- Dispense Underfill
- Cure Underfill
Capillary Underfill Process 2

- Reduces flux residue
  - Solder paste ~50% flux by volume
  - Flux residue ~12% of original paste volume
- Reduced solder joint volume
  - For comparison to assembly with fluxing underfill
- Kester 6502 tacky flux
- 55μm flux depth
Rework – CSP Removal

- Assembly Process 1, No-clean
- Air Vac DSR 24 rework station
- Board was heated to 90°C
- CSP was heated with a nozzle air temperature of 250°C
- CSP was then easily removed with a custom developed hand tool used to gently lift the CSP from one side producing a peeling action

Site after CSP Removal
Clean-up

- A modified dressing tool was used on the Air Vac system to remove the excess solder and most of the epoxy residue
- The remaining epoxy residue was removed with a rotating flat-tipped brush in a Dremel tool
  - An automated tool has been developed

After Site Clean-up
Re-work Times

<table>
<thead>
<tr>
<th>Process</th>
<th>Time (minutes)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSP removal</td>
<td>3</td>
</tr>
<tr>
<td>Dressing with modified</td>
<td>1</td>
</tr>
<tr>
<td>Air Vac Nozzle</td>
<td></td>
</tr>
<tr>
<td>Brushing</td>
<td>2</td>
</tr>
</tbody>
</table>

After rework the sites were inspected. There was some roughening of the solder mask surface, but no solder mask damage (deep scratches, peeling, etc.) was observed. The test vehicles were then re-build using solder paste.
Re-assembly

Capillary Underfill Process

- The stage temperature for dispense was 100°C and a “L” shaped dispense pattern

<table>
<thead>
<tr>
<th>Underfill</th>
<th>Dispense Time (sec.)</th>
<th>Flow Time (sec.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A, with Solder Paste</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>A, Cleaned</td>
<td>5</td>
<td>7</td>
</tr>
<tr>
<td>A, Flux</td>
<td>5</td>
<td>13</td>
</tr>
<tr>
<td>B, As-built</td>
<td>6</td>
<td>3</td>
</tr>
<tr>
<td>B, Reworked</td>
<td>6</td>
<td>3</td>
</tr>
</tbody>
</table>
Fluxing Underfill Process

- 12-hour dehydration bake at 125°C
  - Remove any moisture from the board
  - Ensure the solder mask was fully cured
Initial Placement Results

Placement Voids

- Experiments performed to verify voids not due to:
  - Moisture
  - Solder mask volatiles
  - Underfill outgassing
  - Chemical reactions (fluxing) with the solder balls
Placement Optimization DOE

- Results:
  - Placement force: 1N
  - Placement acceleration: 0.1g
  - Placement dwell time: 3s

‘Optimized’ Placement
Reflow Profile

Good Wetting
Drop Test

- Metal weight (57.5 grams)
- Six foot drop
- Concrete

Results

Failure = 10% increase in resistance
Non-Underfilled failure

Failure with underfill A, solder paste, not cleaned
Liquid-to-Liquid Thermal Shock (-40°C to +125°C)

- 5200 cycles completed
  - One failure (1/30) with Underfill A with Paste @ 3846.5 cycles
  - One failure (1/30) with Underfill B with Paste Reworked @ 312.5 cycles
  - NO failures (0/30) with Underfill A & Flux
  - NO failures (0/30) with Underfill A & Cleaned
  - NO failures (0/30) with Underfill B As-built
  - NO Failures (0/30) with Underfill C
Alternate Underfill Option

- Board does not require dehydration
- No separate cure step
- Reworkable
- Reliability intermediate to full capillary underfill

Guoyun Tian, Yueli Liu, Pradeep Lall, R. Wayne Johnson, Sanan Abderrahman, Mike Palmer, Jeffrey Suhling and Larry Crane, "Corner Bonding of CSPs: Processing and Reliability, Proceedings of the 2003 APEX Conference

Drop Test Results

![Drop Test Results Chart]

- Without underfill
- Corner Dots
- Capillary Underfill

Number of Drops vs. Percent Failures
Video – Drop Test

Modeling
Comparison

4.5 ms After Impact

Comparison

7.5 ms After Impact
Comparison

18 ms After Impact

Lead Free CSP
Test Vehicle

- Four-layer test board
  - 10 CSP attachment sites per side.
  - Only one side was populated.
  - Board was 2.95" by 7.24" by 0.042" thick.
  - The pads were 0.010” in diameter, non-solder mask defined
  - Immersion Ag finish

Test Vehicle

The CSP
- 8mm
- 0.5mm pitch
- 132 I/O
- TapeArray from Amkor Technology.
- 14 x 14 array with only the outer three rows populated.
- CSP was a daisy chain test part for continuity measurements
- Silicon die was 3.98mm x 3.98mm
Assembly

- 4mil thick electropolished, Ni plated, laser cut stencil.
  - The aperture in the stencil was 0.010” square
- No-clean solder paste

Assembly Issues

- Solder Alloys
  - Multicore LF300 lead-free solder paste (95.5%Sn/3.8% Ag/0.7%Cu, type 3)
  - Multicore MP200 63Sn/37Pb, type 3 solder paste
- Lead Free Reflow profile
X-Ray Image of Lead Free Solder

Drop Test Results:
As a Function of Profile
Failure Analysis: As a Function of Profile

Ramp-to-Peak Soak Profile

DSC – Fluxing Underfill

Ramp-to-Peak Lead Free Profile SnPb Profile
Placement Voids

Initial  After process Optimization

Underfill Options

<table>
<thead>
<tr>
<th>Underfill Type</th>
<th>Capillary - A</th>
<th>Capillary - B</th>
<th>Fluxing</th>
<th>Corner Bond</th>
<th>Corner Bond</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solder Alloy</td>
<td>Sn/Ag/Cu &amp; Sn/Pb</td>
<td>Sn/Ag/Cu &amp; Sn/Pb</td>
<td>Sn/Ag/Cu &amp; SnPb</td>
<td>Sn/Pb</td>
<td>Sn/Ag/Cu</td>
</tr>
<tr>
<td>Tg (°C)</td>
<td>110</td>
<td>10</td>
<td>83</td>
<td>122</td>
<td>150</td>
</tr>
<tr>
<td>CTE Below Tg (ppm/°C)</td>
<td>50</td>
<td>83</td>
<td>77</td>
<td>47</td>
<td>60</td>
</tr>
<tr>
<td>CTE Above Tg (ppm/°C)</td>
<td>160</td>
<td>211</td>
<td>190</td>
<td>165</td>
<td>155</td>
</tr>
<tr>
<td>Modulus (MPa)</td>
<td>2069</td>
<td>50</td>
<td>2600</td>
<td>2297</td>
<td>3800</td>
</tr>
</tbody>
</table>
## Placement Offset Summary

<table>
<thead>
<tr>
<th>Offset</th>
<th>No underfill</th>
<th>Fluxing</th>
<th>Corner-bond</th>
</tr>
</thead>
<tbody>
<tr>
<td>X direction 50% offset</td>
<td>good</td>
<td>good</td>
<td>good</td>
</tr>
<tr>
<td>X and Y direction 50% offset</td>
<td>good</td>
<td>good</td>
<td>bad</td>
</tr>
</tbody>
</table>

X-Ray Image of CSP with 50% Off-pad in both the X and Y Directions

---

## 50% in both the X and Y Directions with Corner Bond Underfill

X-Ray Image of CSP with 50% Off-pad in both the X and Y Directions
Drop Test

- Metal weight (31.8 grams)
- Six foot drop
- Concrete
- A 10% increase in resistance was recorded as a failure

Drop Test Results:
As Built

![Graph showing percent failure vs. number of drops for different bond types and underfills.]

- SnPb: No underfill
- SnPb: Corner Bond
- SnPb: Capillary A
- SnPb: Capillary B, 56% beyond 100
- LF: No underfill
- LF: Corner Bond
- LF: Capillary A, 44% beyond 100
- LF: Capillary B, 96% beyond 100
- LF: Fluxing, No Failures at 150
- SnPb Fluxing, 94% beyond 100
Drop Test Results:
125°C Aging

Drop Test Results:
Double Reflow
Failure Analysis: No Underfill

Lead Free Sn/Pb Eutectic

Failure Analysis: Corner Bond

Lead Free Sn/Pb Eutectic
Failure Analysis:
Lead Free, Capillary Underfill – A

Failure Analysis:
Lead Free 125°C Aging

0 Hours

250 Hours
Failure Analysis: Lead Free Double Reflow

1 Reflow

2 Reflows

Reliability - Thermal Cycle
Leadframe Type

Graphs showing failure rate over thermal cycles for different conditions.
CSP PACKAGES

Flex Interposer

µBGA Reliability

Difference in Coefficient of Thermal Expansion Between Silicon (2-3 Ppm/°C) and the PCB (15-20 ppm/°C) Creates Stresses During Thermal Cycling and Leads to Poor Reliability Unless Properly Designed and Compensated for.

Stress Absorbing CSP Device on FR-4 Board
CSP PACKAGES

Flexible Interposer

μBGA Reliability

- Encapsulant optimization for high lead reliability
- Low modulus nubbin for high solder joint reliability

Die Expansion: 3 ppm/°C
Nubbin Deformation
Solder Deformation
Board Expansion: 16 ppm/°C

CSP PACKAGES

Flexible Interposer

μBGA Reliability

Graph showing temperature cycle from -60 to 150°C on board.
CSP PACKAGES
Flex Interposer

μBGA Reliability
Lead Failure Modes

Heel Break
Mid-span Break

CSP PACKAGES
Flex Interposer

μBGA Reliability

Design Parameters
- Lead angle (lead length)
- Heel radius
- Elastomer height
- Lead width variation

Failure Rate vs. Lead Angle

Mid-span
Heel
CSP PACKAGES
Wafer Level Assembly

Flip Chip Technologies - Ultra CSP
Thermal Cycling Reliability

Ultra CSP 65 DOE I

Ultra CSP 65 DOE II

CSP PACKAGES
Wafer Level Assembly

Flip Chip Technologies - Ultra CSP
Thermal Cycling Reliability

Ultra CSP 65 DOE II
CSP PACKAGES
Wafer Level Assembly

Flip Chip Technologies - Ultra CSP
Thermal Cycling Reliability

Smaller Pad on PWB Improves Reliability

CSP PACKAGES
Wafer Level Assembly

Flip Chip Technologies - Ultra CSP
Solder Joint Fatigue Failures
CSP PACKAGES
Wafer Level Assembly

- Liquid to Liquid Thermal Shock
  (-55°-125°C, 5 minute dwell).
- One test board with 8 DCTD die
- Test suspended at 6300 cycles

FormFactor MOST

Type 06 spring
(635μm x 560μm)

CSP PACKAGES
Wafer Level Assembly

- 1000 cycles to failure
- Spring not fully immersed in solder
- Crack around tip of spring
**CSP PACKAGES**
**Wafer Level Assembly**

- Placement is off to the left.
- Note small “front” fillet.

**CSP PACKAGES**
**Wafer Level Assembly**

- Good placement
- Better front fillet
- Cracking around spring
CSP PACKAGES
Wafer Level Assembly

Population 1
- Air to Air temperature cycling
- -40° to 125°C, 10 minute dwell
- Five test boards with 8 test die each
- “Preconditioning” 1000 cycles of -65° to 150°C as an overstress
- Test suspended at 7700 cycles
  - \( \alpha = 7450 \)
  - \( \beta = 6.3 \)

Population 2
- Air to Air temperature cycling
- -40° to 125°C, 10 minute dwell
- 8 test boards with 8 test die each
- Test suspended at 9600 cycles
  - \( \alpha = 10010 \)
  - \( \beta = 8.5 \)

Summary

- CSPs are gaining in popularity, especially for portable electronics.
- Pitch will get smaller (assembly/substrates more difficult) as higher I/O count devices are incorporated.
- For harsh environments including mechanical shock & bend, underfill may be required.