# JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech. (EMBEDDED SYSTEMS & VLSI DESIGN/VLSI AND EMBEDDED SYSTEMS/ELECTRONICS DESIGN TECHNOLOGY)

## COURSE STRUCTURE AND SYLLABUS

### I Year – I Semester

<table>
<thead>
<tr>
<th>Category</th>
<th>Course Title</th>
<th>Int. marks</th>
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<tr>
<td>Core Course I</td>
<td>Embedded System Design</td>
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<td>Open Elective I</td>
<td>Network Security and Cryptography</td>
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EMBEDDED SYSTEM DESIGN

UNIT - I:
Introduction to Embedded Systems

UNIT - II:
Typical Embedded System:
Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT - III:
Embedded Firmware:
Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT - IV:
RTOS Based Embedded System Design:
Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT - V:
Task Communication:
Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:
1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

REFERENCE BOOKS:
1. Embedded Systems - Raj Kamal, TMH.
4. An Embedded Software Primer - David E. Simon, Pearson Education.
VLSI TECHNOLOGY

UNIT –I:
Review of Microelectronics and Introduction to MOS Technologies:
MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits:
I ds – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi
CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II:
Layout Design and Tools:
Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.
Logic Gates & Layouts:
Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and
Inductive interconnect delays.

UNIT –III:
Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal
growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic
wafer fabrication operations, Yield measurement, Contamination sources, Clean room construction,
Oxidation and Photolithography, Doping and Depositions, Metallization. Ten step patterning process,
Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking
process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping

UNIT –IV
Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1,
Ion implantation-2, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced
CVD systems, Vapour phase epitoxy, molecular beam epitaxy.

UNIT –V
Design rules and Scaling, BICMOS ICs: Choice of transistor types, pnp transistors, Resistors,
capacitors,
Packaging: Chip characteristics, package functions, package operations

Text Books:

Reference Books:
   Learning2011.
2. Eugene D. Fabricius, Introduction to VLSI design, McGraw Hill, 1999
CMOS ANALOG INTEGRATED CIRCUIT DESIGN

UNIT -I:
MOS Devices and Modeling:

UNIT -II:
Analog CMOS Sub-Circuits:
MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -III:
CMOS Amplifiers:
Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT -IV:
CMOS Operational Amplifiers:

UNIT -V:
Comparators:
Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

REFERENCE BOOKS:
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.
UNIT –I:
Co-Design Issues:
Co-Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co-Synthesis Algorithms:
Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II:
Prototyping and Emulation:
Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures:
Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III:
Compilation Techniques and Tools for Embedded Processor Architectures:
Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV:
Design Specification and Verification:
Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V:
Languages for System – Level Specification and Design-I:
System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II:
Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

REFERENCE BOOKS:
1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont -2010 – Springer
UNIT -I:
Minimization and Transformation of Sequential Machines:
The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine
minimization – Simplification of incompletely specified machines.
Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles
and Hazards.

UNIT -II:
Digital Design:
Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control
circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner,
Binary divider.

UNIT -III:
SM Charts:
State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary
Multiplier, dice game controller.

UNIT -IV:
Fault Modeling & Test Pattern Generation:
Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault
dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.
Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques,
Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random
testing, Transition count testing, Signature analysis and test bridging faults.

UNIT -V:
Fault Diagnosis in Sequential Circuits:
Circuit Test Approach, Transition Check Approach – State identification and fault detection
experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A.
   Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI

REFERENCE BOOKS:
UNIT- I:
Fundamentals of Computer Design

UNIT – II: Pipelines
Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties.
Memory Hierarchy Design

UNIT - III: Instruction Level Parallelism the Hardware Approach
Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.
ILP Software Approach
Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT – IV:
Multi Processors and Thread Level Parallelism
Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT – V:
Inter Connection and Networks
Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.
Intel Architecture
Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOKS:

REFERENCE BOOKS:
2. Computer Architecture and Parallel Processing ,Kai Hwang, Faye A.Brigs., MC Graw Hill,
UNIT I
Essential feature of Instruction set architectures of CISC, RISC and DSP processors and their implications for implementation as VLSI Chips, Micro programming approaches for implementation of control part of the processor. Assessing understanding performance, Introduction, CPU performance and its factors, evaluating performance, real stuff: Two spec bench marks and performance of recent INTEL processors, fallacies and pitfalls

UNIT II
Data Path and Control: Introduction, logic design conventions, building a data path, a simple implementation scheme, a multi cycle implementation, exceptions, micro programming: simplifying control design, an introduction to digital design using hardware description language, fallacies and pitfalls

UNIT III
Enhancing performance with pipeline: An overview of pipelining, a pipe lined data path. Pipe lined control, data hazards and forwarding, data hazards and stalls, branch hazards using a hard ware description language to describe and model a pipe line, exceptions, advanced pipelining: extracting more performance, fallacies and pitfalls

UNIT IV
Computational Accuracy in DSP implementations: Introduction, number formats for signals and coefficients in DSP system, dynamic range and precision, sources of errors in DSP implementations, A/D conversion errors, DSP computational errors, D /A conversion errors

UNIT V
Architectures for programmable digital signal processing devices: introduction, basic architectural features, DSP Computational building blocks, bus architecture and memory, data addressing capabilities, address generation unit, programmability and program execution, speed issues, features for external interfacing.

Text books:

Reference Books:
2. Keshab Parhi, VLSI Digital Signal Processing system design and implementations, Wiley 1999
CMOS DIGITAL INTEGRATED CIRCUIT DESIGN
(Core Elective –II)

UNIT –I:
MOS Design:
Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT –II:
Combinational MOS Logic Circuits:
MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT –III:
Sequential MOS Logic Circuits:
Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flipflop.

UNIT –IV:
Dynamic Logic Circuits:
Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT –V:
Semiconductor Memories:
Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

TEXT BOOKS:

REFERENCE BOOKS:
UNIT-I:
Introduction to Programmable Logic Devices:

UNIT-II:
Field Programmable Gate Arrays:
Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III:
SRAM Programmable FPGAs:

UNIT -IV:
Anti-Fuse Programmed FPGAs:
Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V:
Design Applications:
General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

REFERENCE BOOKS:
1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
UNIT –I:
Modern Techniques: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

UNIT -II:
Conventional Encryption: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.

UNIT -III:
Number Theory: Prime and Relatively prime numbers, Modular arithmetic, Fermat’s and Euler’s theorems, Testing for primality, Euclid’s Algorithm, the Chinese remainder theorem, Discrete logarithms.

UNIT -IV:
Hash and Mac Algorithms: MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC.
Authentication Applications: Kerberos, X.509 directory Authentication service.
Electronic Mail Security: Pretty Good Privacy, S/MIME.

UNIT –V:
Intruders, Viruses and Worms: Intruders, Viruses and Related threats.
Fire Walls: Fire wall Design Principles, Trusted systems.

TEXT BOOKS:

REFERENCE BOOKS:
5. Introduction to Cryptography - Buchmann, Springer.
ADVANCED DATA COMMUNICATIONS
(Open Elective – I)

Unit I
Data Communications, Networks and Network Types, Internet History, Standards and Administration,

Data Link Layer
Introduction, Data Link Layer, Nodes and Links, Services, Categories of Links, sub layers, Link
Layer Addressing, Address Resolution Protocol.

Unit II
Error Detection and Correction: Types of Errors, Redundancy, detection versus correction, Coding
Block Coding: Error Detection, Vertical redundancy checks, longitudinal redundancy checks, Error
Correction, Error correction single bit, Hamming code.
Cyclic Codes: Cyclic Redundancy Check, Polynomials, Cyclic Code Encoder Using Polynomials,
Cyclic Code Analysis, Advantage of Cyclic Codes, Checksum
Data Link Control: DLC Services, Data Link Layer Protocols, HDLC, Point to Point Protocol

Unit III
Switching: Introduction to Switching, Circuit Switched Networks, Packet Switching, Structure of
switch
Multiplexing: Multiplexing, Frequency Division Multiplexing, Time Division Multiplexing.
Connecting devices: Passive Hubs, Repeaters, Active Hubs, Bridges, Two Layer Switches, Routers,
Three Layer Switches, Gateway, Backbone Networks.
Wired LANS: Ethernet Protocol, Standard Ethernet, Fast Ethernet, Gigabit Ethernet, 10 Giga bit
Ethernet

Unit IV
Media Access Control (MAC) Sub Layer
Random Access, ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with
Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance
(CSMA/CA), Controlled Access- Reservation, Polling- Token Passing, Channelization - Frequency
Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), Code - Division Multiple
Access (CDMA).
Spectrum Spreading: Spread Spectrum-Frequency Hopping Spread Spectrum and Direct Sequence
Spread Spectrum.

Unit V
Networks Layer: Packetizing, Routing and Forwarding, Packet Switching, Network Layer
Performance, IPv4 Address, Address Space, Classful Addressing, Classless Addressing, Dynamic
Host Configuration Protocol (DHCP), Network Address Resolution (NATF), Forwarding of IP Packets,
Forwarding based on Destination Address, Forwarding based on Label, Routing as Packet Switches.
Unicast Routing: Introduction, Routing Algorithms-Distance Vector Routing, Link State Routing,
Path Vector Routing, Unicast Routing Protocols- Routing Information Protocol (RIP), Open Short
Path First Version 4.

TEXT BOOKS:
1. Data Communications and Networking - B. A. Forouzan, 5th, 2013, TMH.

REFERENCE BOOKS:
1. Data Communications and Computer Networks - Prakash C. Gupta, 2006, PHI.
2. Data Communications and Networking - B. A. Forouzan, 2nd, 2013, TMH.
SOFT COMPUTING TECHNIQUES
(Open Elective –I)

UNIT – I: Fundamentals of Neural Networks & Feed Forward Networks

Basic Concept of Neural Networks, Human Brain, Models of an Artificial Neuron, Learning Methods, Neural Networks Architectures, Signal Layer Feed Forward Neural Network: The Perceptron Model, Multilayer Feed Forward Neural Network, Architecture of a Back Propagation Network (BPN), The Solution, Backpropagation Learning, Selection of various Parameters in BPN. Application of Backpropagation Networks in Pattern Recognition & Image Processing.

UNIT – II: Associative Memories & ART Neural Networks

Basic concepts of Linear Associator, Basic concepts of Dynamical systems, Mathematical Foundation of Discrete-Time Hop field Networks (HPF), Mathematical Foundation of Gradient-Type Hopfield Networks, Transient response of Continuous Time Networks, Applications of HPF in Solution of Optimization Problem: Minimization of the Traveling salesman tour length, Summing networks with digital outputs, Solving Simultaneous Linear Equations, Bidirectional Associative Memory Networks; Cluster Structure, Vector Quantization, Classical ART Networks, Simplified ART Architecture.

UNIT – III: Fuzzy Logic & Systems

Fuzzy sets, Crisp Relations, Fuzzy Relations, Crisp Logic, Predicate Logic, Fuzzy Logic, Fuzzy Rule based system, Defuzzification Methods, Applications: Greg Viot’s Fuzzy Cruise Controller, Air Conditioner Controller.

UNIT – IV: Genetic Algorithms


UNIT – V: Hybrid Systems


TEXT BOOKS:
1. Introduction to Artificial Neural Systems - J.M.Zurada, Jaico Publishers

REFERENCE BOOKS:
1. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.
JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

VLSI LABORATORY

Note:
- Minimum of 10 programs from Part –I and 2 programs from Part -II are to be conducted.

Design and implementation of the following CMOS digital/analog circuits using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools. The design shall include Gate-level design, Transistor-level design, Hierarchical design, Verilog HDL/VHDL design, Logic synthesis, Simulation and verification.

Part –I: VLSI Front End Design programs:
Programming can be done using any compiler. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Design of 2-to-4 decoder
4. Design of 8-to-3 encoder (without and with parity)
5. Design of 8-to-1 multiplexer
6. Design of 4 bit binary to gray converter
7. Design of Multiplexer/ Demultiplexer, comparator
8. Design of Full adder using 3 modeling styles
9. Design of flip flops: SR, D, JK, T
10. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
12. Design of Sequence Detector (Finite State Machine-Mealy and Moore Machines).
13. Design of 4-Bit Multiplier, Divider.
14. Design of ALU to Perform – ADD, SUB, AND-OR, 1’s and 2’s Compliment, Multiplication, and Division.
15. Design of Finite State Machine.
16. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits.

Part –II: VLSI Back End Design programs:
Design and implementation of the following CMOS digital/analog circuits using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools. The design shall include Gate-level design/Transistor-level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:
   - Basic logic gates
   - CMOS inverter
   - CMOS NOR/ NAND gates
   - CMOS XOR and MUX gates
   - CMOS 1-bit full adder
   - Static / Dynamic logic circuit (register cell)
   - Latch
   - Pass transistor
3. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths