**FEATURES**

- **Input voltage range:** 3.3 V to 20 V
- **Maximum output current:** 300 mA
- **Low noise:** 15 μV rms for fixed output versions
- **PSRR performance:** 60 dB at 10 kHz, \( V_{OUT} = 3.3 \) V
- **Reverse current protection**
- **Low dropout voltage:** 200 mV at 300 mA load
- **Initial accuracy:** ±0.8%
- **Accuracy over line, load, and temperature:** −2%, +1%
- **Stable with small 1 μF ceramic output capacitor**
- **7 fixed output voltage options:** 1.5 V, 1.8 V, 2.5 V, 3 V, 3.3 V, 5 V, and 9 V
- **Adjustable output from 1.22 V to \( V_{IN} - V_{DO} \)**
- **Foldback current limit and thermal overload protection**
- **User programmable precision UVLO/enable**
- **Power-good indicator**
- **8-lead LFCSP and 8-lead SOIC packages**

**APPLICATIONS**

- Regulation to noise sensitive applications: ADC, DAC circuits, precision amplifiers, high frequency oscillators, clocks, and phase-locked loops
- Communications and infrastructure
- Medical and healthcare
- Industrial and instrumentation

**GENERAL DESCRIPTION**

The ADP7102 is a CMOS, low dropout linear regulator that operates from 3.3 V to 20 V and provides up to 300 mA of output current. This high input voltage LDO is ideal for regulation of high performance analog and mixed signal circuits operating from 19 V to 1.22 V rails. Using an advanced proprietary architecture, it provides high power supply rejection, low noise, and achieves excellent line and load transient response with just a small 1 μF ceramic output capacitor.

The ADP7102 is available in seven fixed output voltage options and an adjustable version, which allows output voltages that range from 1.22 V to \( V_{IN} - V_{DO} \) via an external feedback divider.

The ADP7102 output noise voltage is 15 μV rms and is independent of the output voltage. A digital power-good output allows power system monitors to check the health of the output voltage. A user programmable precision undervoltage lockout function facilitates sequencing of multiple power supplies.

The ADP7102 is available in 8-lead, 3 mm × 3 mm LFCSP and 8-lead SOIC packages. The LFCSP offers a very compact solution and also provides excellent thermal performance for applications requiring up to 300 mA of output current in a small, low profile footprint.
Comparable Parts
View a parametric search of comparable parts

Evaluation Kits
• ADP7102 Evaluation Board

Documentation
Application Notes
• AN-1316: Generating Multiple Isolated Bias Rails for IGBT Motor Drives with Flyback, SEPIC, and Ćuk Combination
• AN-1329: Noise Reduction Network for Adjustable Low Dropout Regulators

Data Sheet
• ADP7102: 20 V, 300 mA, Low Noise, CMOS LDO Data Sheet

User Guides
• UG-218: User Guide for the ADP7102/ADP7104 Evaluation Board
• UG-264: RedyKits for the ADP7102 Low Dropout (LDO) Linear Regulator
• UG-582: Evaluating the EVAL-CN0290-SDPZ

Tools and Simulations
• ADI Linear Regulator Design Tool and Parametric Search
• ADIsimPower™ Voltage Regulator Design Tool

Reference Designs
• CN0075
• CN0281
• CN0290
• CN0292
• CN0373

Reference Materials
Solutions Bulletins & Brochures
• Ultralow Noise, High Rejection Low Dropout Regulators

Design Resources
• ADP7102 Material Declaration
• PCN-PDN Information
• Quality And Reliability
• Symbols and Footprints

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# ADP7102 Data Sheet

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## REVISION HISTORY

- 9/15—Rev. D to Rev. E
  Changes to Figure 60 ...................................................................... 17

- 5/14—Rev. C to Rev. D
  Changed UVLO Threshold Rising Typ Parameter from 1.23 V to 1.22 V; Table 1 ................................................................. 4
  Changes to Power Good Section .................................................. 20
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- 8/13—Rev. B to Rev. C
  Changes to Table 3 ............................................................................ 5

  Changes to Noise Reduction of the Adjustable ADP7102 Section ................................................................. 20

- 11/11—Rev. 0 to Rev. A
  Changes to Figure 50 ...................................................................... 14

- 10/11—Revision 0: Initial Version
**SPECIFICATIONS**

\( V_{IN} = (V_{OUT} + 1 \text{ V}) \) or 3.3 V (whichever is greater), \( EN = V_{IN}, I_{OUT} = 10 \text{ mA}, C_{IN} = C_{OUT} = 1 \mu \text{F}, T_{A} = 25°C, \) unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>INPUT VOLTAGE RANGE</strong></td>
<td>( V_{IN} )</td>
<td>( I_{OUT} = 100 \mu \text{A}, V_{IN} = 10 \text{ V} )</td>
<td>3.3</td>
<td>20</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td><strong>OPERATING SUPPLY CURRENT</strong></td>
<td>( I_{GND} )</td>
<td>( I_{OUT} = 100 \mu \text{A}, V_{IN} = 10 \text{ V}, T_{J} = −40°C ) to +125°C</td>
<td>400</td>
<td>900</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{OUT} = 10 \text{ mA}, V_{IN} = 10 \text{ V} )</td>
<td>450</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{OUT} = 10 \text{ mA}, V_{IN} = 10 \text{ V}, T_{J} = −40°C ) to +125°C</td>
<td>1050</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{OUT} = 150 \text{ mA}, V_{IN} = 10 \text{ V} )</td>
<td>650</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{OUT} = 150 \text{ mA}, V_{IN} = 10 \text{ V}, T_{J} = −40°C ) to +125°C</td>
<td>1250</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{OUT} = 300 \text{ mA}, V_{IN} = 10 \text{ V} )</td>
<td>750</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{OUT} = 300 \text{ mA}, V_{IN} = 10 \text{ V}, T_{J} = −40°C ) to +125°C</td>
<td>1400</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td><strong>SHUTDOWN CURRENT</strong></td>
<td>( I_{GND-SD} )</td>
<td>( EN = GND, V_{IN} = 12 \text{ V} )</td>
<td>40</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( EN = GND, V_{IN} = 12 \text{ V}, T_{J} = −40°C ) to +125°C</td>
<td>75</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td><strong>INPUT REVERSE CURRENT</strong></td>
<td>( I_{REV-INPUT} )</td>
<td>( EN = GND, V_{IN} = 0 \text{ V}, V_{OUT} = 20 \text{ V} )</td>
<td>0.3</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( EN = GND, V_{IN} = 0 \text{ V}, V_{OUT} = 20 \text{ V}, T_{J} = −40°C ) to +125°C</td>
<td>5</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td><strong>OUTPUT VOLTAGE ACCURACY</strong></td>
<td>( V_{OUT} )</td>
<td>( I_{OUT} = 10 \text{ mA} )</td>
<td></td>
<td>−0.8</td>
<td>+0.8</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 1 \text{ mA} &lt; I_{OUT} &lt; 300 \text{ mA}, V_{IN} = (V_{OUT} + 1 \text{ V}) ) to 20 V, ( T_{J} = −40°C ) to +125°C</td>
<td></td>
<td>−2</td>
<td>+1</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{OUT} = 10 \text{ mA} )</td>
<td>1.21</td>
<td>1.22</td>
<td>1.23</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 1 \text{ mA} &lt; I_{OUT} &lt; 300 \text{ mA}, V_{IN} = (V_{OUT} + 1 \text{ V}) ) to 20 V, ( T_{J} = −40°C ) to +125°C</td>
<td>1.196</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td><strong>LINE REGULATION</strong></td>
<td>( \Delta V_{OUT} / \Delta V_{IN} )</td>
<td>( V_{IN} = (V_{OUT} + 1 \text{ V}) ) to 20 V, ( T_{J} = −40°C ) to +125°C</td>
<td>−0.015</td>
<td></td>
<td>+0.015</td>
<td>%/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{OUT} = 1 \text{ mA} ) to 300 mA</td>
<td>0.2</td>
<td></td>
<td>0.015</td>
<td>%/A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{OUT} = 1 \text{ mA} ) to 300 mA, ( T_{J} = −40°C ) to +125°C</td>
<td>1.0</td>
<td></td>
<td>1.0</td>
<td>%/A</td>
</tr>
<tr>
<td><strong>LOAD REGULATION</strong></td>
<td>( \Delta V_{OUT} / \Delta I_{OUT} )</td>
<td>( 1 \text{ mA} &lt; I_{OUT} &lt; 300 \text{ mA}, V_{IN} = (V_{OUT} + 1 \text{ V}) ) to 20 V, ADJ connected to VOUT</td>
<td>10</td>
<td></td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 1 \text{ mA} &lt; I_{OUT} &lt; 300 \text{ mA}, V_{IN} = (V_{OUT} + 1 \text{ V}) ) to 20 V, SENSE connected to VOUT, ( V_{OUT} = 1.5 \text{ V} )</td>
<td>1</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td><strong>ADJ INPUT BIAS CURRENT</strong></td>
<td>( \text{ADJ}_{-\text{BIAS}} )</td>
<td>( 1 \text{ mA} &lt; I_{OUT} &lt; 300 \text{ mA}, V_{IN} = (V_{OUT} + 1 \text{ V}) ) to 20 V, ADJ connected to VOUT</td>
<td>10</td>
<td></td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td><strong>SENSE INPUT BIAS CURRENT</strong></td>
<td>( \text{SENSE}_{-\text{BIAS}} )</td>
<td>( 1 \text{ mA} &lt; I_{OUT} &lt; 300 \text{ mA}, V_{IN} = (V_{OUT} + 1 \text{ V}) ) to 20 V, SENSE connected to VOUT, ( V_{OUT} = 1.5 \text{ V} )</td>
<td>1</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td><strong>DROPOUT VOLTAGE</strong></td>
<td>( V_{DROPOUT} )</td>
<td>( I_{OUT} = 10 \text{ mA} )</td>
<td>20</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{OUT} = 10 \text{ mA}, T_{J} = −40°C ) to +125°C</td>
<td>40</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{OUT} = 150 \text{ mA} )</td>
<td>100</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{OUT} = 150 \text{ mA}, T_{J} = −40°C ) to +125°C</td>
<td>175</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{OUT} = 300 \text{ mA} )</td>
<td>200</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{OUT} = 300 \text{ mA}, T_{J} = −40°C ) to +125°C</td>
<td>325</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td><strong>START-UP TIME</strong></td>
<td>( t_{\text{START-UP}} )</td>
<td>( V_{OUT} = 5 \text{ V} )</td>
<td>800</td>
<td></td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td><strong>CURRENT-LIMIT THRESHOLD</strong></td>
<td>( I_{\text{LIMIT}} )</td>
<td></td>
<td>450</td>
<td>575</td>
<td>750</td>
<td>mA</td>
</tr>
<tr>
<td><strong>PG OUTPUT LOGIC LEVEL</strong></td>
<td>( \text{PG}_{\text{HIGH}} )</td>
<td>( I_{CH} &lt; 1 \mu \text{A} )</td>
<td>1.0</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{OL} &lt; 2 \mu \text{A} )</td>
<td>0.4</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td><strong>PG OUTPUT THRESHOLD</strong></td>
<td>( \text{PG}_{\text{FALL}} )</td>
<td>( \text{PG}_{\text{RISE}} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\[ t_{\text{START-UP}} = \frac{V_{OUT}}{I_{\text{LIMIT}}} \]

\[ I_{\text{LIMIT}} = \frac{V_{OUT}}{t_{\text{START-UP}}} \]
## THERMAL SHUTDOWN

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Shutdown Threshold</td>
<td>TS(_{SD})</td>
<td>(T_J) rising</td>
<td>150</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Thermal Shutdown Hysteresis</td>
<td>TS(_{SD-HYS})</td>
<td></td>
<td>15</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

## PROGRAMMABLE EN/UVLO

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>UVLO Threshold rising</td>
<td>UVLO(_{RISE})</td>
<td>(3.3 \leq V_{IN} \leq 20) V, (T_J = -40°C) to +125°C</td>
<td>1.18</td>
<td>1.22</td>
<td>1.28</td>
<td>V</td>
</tr>
<tr>
<td>UVLO Threshold falling</td>
<td>UVLO(_{FALL})</td>
<td>(3.3 \leq V_{IN} \leq 20) V, (T_J = -40°C) to +125°C, 10 kΩ in series with enable pin</td>
<td>1.13</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>UVLO Hysteresis Current Enable Pulldown Current</td>
<td>UVLO(<em>{HYS}), (I</em>{EN-IN})</td>
<td>(V_{EN} &gt; 1.25) V, (T_J = -40°C) to +125°C</td>
<td>7.5</td>
<td>9.8</td>
<td>12</td>
<td>μA</td>
</tr>
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</table>

## INPUT VOLTAGE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start Threshold</td>
<td>(V_{START})</td>
<td>(T_J = -40°C) to +125°C</td>
<td>3.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Shutdown Threshold Hysteresis</td>
<td>(V_{SHUTDOWN})</td>
<td>(T_J = -40°C) to +125°C</td>
<td>2.45</td>
<td>250</td>
<td></td>
<td>mV</td>
</tr>
</tbody>
</table>

## OUTPUT NOISE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Rejection Ratio</td>
<td>PSRR</td>
<td>100 kHz, (V_{IN} = 4.3) V, (V_{OUT} = 3.3) V</td>
<td>50</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

## POWER SUPPLY REJECTION RATIO

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dropout Voltage</td>
<td></td>
<td>100 kHz, (V_{IN} = 6) V, (V_{OUT} = 5) V</td>
<td>50</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td></td>
<td>10 kHz, (V_{IN} = 4.3) V, (V_{OUT} = 3.3) V</td>
<td>60</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td></td>
<td>10 kHz, (V_{IN} = 6) V, (V_{OUT} = 5) V</td>
<td>60</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td></td>
<td>100 kHz, (V_{IN} = 3.3) V, (V_{OUT} = 1.8) V, adjustable mode</td>
<td>50</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td></td>
<td>100 kHz, (V_{IN} = 6) V, (V_{OUT} = 5) V, adjustable mode</td>
<td>60</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td></td>
<td>100 kHz, (V_{IN} = 16) V, (V_{OUT} = 15) V, adjustable mode</td>
<td>60</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td></td>
<td>10 kHz, (V_{IN} = 3.3) V, (V_{OUT} = 1.8) V, adjustable mode</td>
<td>60</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td></td>
<td>10 kHz, (V_{IN} = 6) V, (V_{OUT} = 5) V, adjustable mode</td>
<td>60</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td></td>
<td>10 kHz, (V_{IN} = 16) V, (V_{OUT} = 15) V, adjustable mode</td>
<td>60</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

---

1 Based on an end point calculation using 1 mA and 300 mA loads. See Figure 6 for typical load regulation performance for loads less than 1 mA.
2 Dropout voltage is defined as the input to output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 3.0 V.
3 Start-up time is defined as the time between the rising edge of EN to VOUT being at 90% of its nominal value.
4 Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 5.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 5.0 V, or 4.5 V.

## INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

### Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Input and Output Capacitance(^1)</td>
<td>(C_{\text{MIN}})</td>
<td>(T_A = -40°C) to +125°C</td>
<td>0.7</td>
<td></td>
<td></td>
<td>μF</td>
</tr>
<tr>
<td>Capacitor ESR</td>
<td>(R_{ESR})</td>
<td>(T_A = -40°C) to +125°C</td>
<td>0.001</td>
<td>0.2</td>
<td></td>
<td>Ω</td>
</tr>
</tbody>
</table>

--

\(^1\) The minimum input and output capacitance should be greater than 0.7 μF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO.

---

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Table 3. ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN to GND</td>
<td>−0.3 V to +22 V</td>
</tr>
<tr>
<td>VOUT to GND</td>
<td>−0.3 V to +20 V</td>
</tr>
<tr>
<td>EN/UVLO to GND</td>
<td>−0.3 V to VIN</td>
</tr>
<tr>
<td>PG to GND</td>
<td>−0.3 V to VIN</td>
</tr>
<tr>
<td>SENSE/ADJ to GND</td>
<td>−0.3 V to VOUT</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
</tr>
<tr>
<td>Operating Junction Temperature Range</td>
<td>−40°C to +125°C</td>
</tr>
<tr>
<td>Soldering Conditions</td>
<td>JEDEC J-STD-020</td>
</tr>
</tbody>
</table>

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP7102 can be damaged when the junction temperature limit is exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated.

In applications with moderate power dissipation and low printed circuit board (PCB) thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction to ambient thermal resistance of the package (θ_JA).

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

\[ T_J = T_A + (P_D \times \theta_{JA}) \]

\[ T_J = T_B + (P_D \times \Psi_{JB}) \]

See JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

Thermal Resistance

θ_{JA} and Ψ_{JB} are specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages. θ_{JC} is a parameter for surface-mount packages with top mounted heat sinks. θ_{JC} is presented here for reference only.

Table 4. Thermal Resistance

<table>
<thead>
<tr>
<th>Package Type</th>
<th>θ_{JA}</th>
<th>θ_{JC}</th>
<th>Ψ_{JB}</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-Lead LFCSP</td>
<td>40.1</td>
<td>27.1</td>
<td>17.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>8-Lead SOIC</td>
<td>48.5</td>
<td>58.4</td>
<td>31.3</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 5. Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VOUT</td>
<td>Regulated Output Voltage. Bypass VOUT to GND with a 1 μF or greater capacitor.</td>
</tr>
<tr>
<td>2</td>
<td>SENSE/ADJ</td>
<td>Sense (SENSE). Measures the actual output voltage at the load and feeds it to the error amplifier. Connect SENSE as close as possible to the load to minimize the effect of IR drop between the regulator output and the load. This function applies to fixed voltages only. Adjust Input (ADJ). An external resistor divider sets the output voltage. This function applies to adjustable voltages only.</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Ground.</td>
</tr>
<tr>
<td>4</td>
<td>NC</td>
<td>Do Not Connect to this Pin.</td>
</tr>
<tr>
<td>5</td>
<td>EN/UVLO</td>
<td>Enable Input (EN). Drive EN high to turn on the regulator; drive EN low to turn off the regulator. Programmable Undervoltage Lockout (UVLO). When the programmable UVLO function is used, the upper and lower thresholds are determined by the programming resistors.</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td>Ground.</td>
</tr>
<tr>
<td>7</td>
<td>PG</td>
<td>Power Good. This open-drain output requires an external pull-up resistor to VIN or VOUT. If the device is in shutdown, current limit, thermal shutdown, or falls below 90% of the nominal output voltage, PG immediately transitions low. If the power-good function is not used, the pin may be left open or connected to ground.</td>
</tr>
<tr>
<td>8</td>
<td>VIN</td>
<td>Regulator Input Supply. Bypass VIN to GND with a 1 μF or greater capacitor.</td>
</tr>
<tr>
<td></td>
<td>EPAD</td>
<td>Exposed Pad. Exposed paddle on the bottom of the package. The EPAD enhances thermal performance and is electrically connected to GND inside the package. It is highly recommended that the EPAD be connected to the ground plane on the board.</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 5\, V$, $V_{OUT} = 3.3\, V$, $I_{OUT} = 1\, mA$, $C_{IN} = C_{OUT} = 1\, \mu F$, $T_A = 25^\circ C$, unless otherwise noted.

Figure 5. Output Voltage vs. Junction Temperature

Figure 6. Output Voltage vs. Load Current

Figure 7. Output Voltage vs. Input Voltage

Figure 8. Ground Current vs. Junction Temperature

Figure 9. Ground Current vs. Load Current

Figure 10. Ground Current vs. Input Voltage
**Figure 11.** Shutdown Current vs. Temperature at Various Input Voltages

**Figure 12.** Dropout Voltage vs. Load Current

**Figure 13.** Output Voltage vs. Input Voltage (in Dropout)

**Figure 14.** Ground Current vs. Input Voltage (in Dropout)

**Figure 15.** Output Voltage vs. Junction Temperature, \( V_{OUT} = 5 \, V \)

**Figure 16.** Output Voltage vs. Load Current, \( V_{OUT} = 5 \, V \)
Figure 23. Ground Current vs. Input Voltage (in Dropout), V_{out} = 5 V

Figure 24. Output Voltage vs. Junction Temperature, V_{out} = 1.8 V

Figure 25. Output Voltage vs. Load Current, V_{out} = 1.8 V

Figure 26. Output Voltage vs. Input Voltage, V_{out} = 1.8 V

Figure 27. Ground Current vs. Junction Temperature, V_{out} = 1.8 V

Figure 28. Ground Current vs. Load Current, V_{out} = 1.8 V
Figure 29. Ground Current vs. Input Voltage, V_{OUT} = 1.8 V

Figure 30. Output Voltage vs. Junction Temperature, V_{OUT} = 5 V, Adjustable

Figure 31. Output Voltage vs. Load Current, V_{OUT} = 5 V, Adjustable

Figure 32. Output Voltage vs. Input Voltage, V_{OUT} = 5 V, Adjustable

Figure 33. Reverse Input Current vs. Temperature, V_{IN} = 0 V, Different Voltages on V_{OUT}

Figure 34. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 1.8 V, V_{IN} = 3.3 V
Figure 35. Power Supply Rejection Ratio vs. Frequency, \( V_{OUT} = 3.3 \) V, \( V_{IN} = 4.8 \) V

Figure 36. Power Supply Rejection Ratio vs. Frequency, \( V_{OUT} = 3.3 \) V, \( V_{IN} = 4.3 \) V

Figure 37. Power Supply Rejection Ratio vs. Frequency, \( V_{OUT} = 3.3 \) V, \( V_{IN} = 3.8 \) V

Figure 38. Power Supply Rejection Ratio vs. Frequency, \( V_{OUT} = 5 \) V, \( V_{IN} = 6.5 \) V

Figure 39. Power Supply Rejection Ratio vs. Frequency, \( V_{OUT} = 5 \) V, \( V_{IN} = 6 \) V

Figure 40. Power Supply Rejection Ratio vs. Frequency, \( V_{OUT} = 5 \) V, \( V_{IN} = 5.5 \) V
Figure 41. Power Supply Rejection Ratio vs. Frequency, $V_{\text{OUT}} = 5 \, V$, $V_{\text{IN}} = 5.3 \, V$

Figure 42. Power Supply Rejection Ratio vs. Frequency, $V_{\text{OUT}} = 5 \, V$, $V_{\text{IN}} = 5.2 \, V$

Figure 43. Power Supply Rejection Ratio vs. Frequency, $V_{\text{OUT}} = 5 \, V$, $V_{\text{IN}} = 6 \, V$, Adjustable

Figure 44. Power Supply Rejection Ratio vs. Frequency, $V_{\text{OUT}} = 5 \, V$, $V_{\text{IN}} = 6 \, V$, Adjustable with Noise Reduction Circuit

Figure 45. Power Supply Rejection Ratio vs. Headroom Voltage, 100 Hz, $V_{\text{OUT}} = 5 \, V$

Figure 46. Power Supply Rejection Ratio vs. Headroom Voltage, 1 kHz, $V_{\text{OUT}} = 5 \, V$
Figure 47. Power Supply Rejection Ratio vs. Headroom Voltage, 10 kHz, $V_{OUT} = 5\, V$

Figure 48. Power Supply Rejection Ratio vs. Headroom Voltage, 100 kHz, $V_{OUT} = 5\, V$

Figure 49. Output Noise vs. Load Current and Output Voltage, $C_{OUT} = 1\, \mu F$

Figure 50. Output Noise Spectral Density, $I_{LOAD} = 10\, mA$, $C_{OUT} = 1\, \mu F$

Figure 51. Load Transient Response, $C_{IN}, C_{OUT} = 1\, \mu F$, $I_{LOAD} = 1\, mA$ to $300\, mA$, $V_{OUT} = 1.8\, V$, $V_{IN} = 5\, V$

Figure 52. Load Transient Response, $C_{IN}, C_{OUT} = 1\, \mu F$, $I_{LOAD} = 1\, mA$ to $300\, mA$, $V_{OUT} = 3.3\, V$, $V_{IN} = 5\, V$
Figure 53. Load Transient Response, C\textsubscript{IN}, C\textsubscript{OUT} = 1 μF, I\textsubscript{LOAD} = 1 mA to 300 mA, V\textsubscript{OUT} = 5 V, V\textsubscript{IN} = 7 V

Figure 54. Line Transient Response, C\textsubscript{IN}, C\textsubscript{OUT} = 1 μF, I\textsubscript{LOAD} = 300 mA, V\textsubscript{OUT} = 1.8 V

Figure 55. Line Transient Response, C\textsubscript{IN}, C\textsubscript{OUT} = 1 μF, I\textsubscript{LOAD} = 300 mA, V\textsubscript{OUT} = 3.3 V

Figure 56. Line Transient Response, C\textsubscript{IN}, C\textsubscript{OUT} = 1 μF, I\textsubscript{LOAD} = 300 mA, V\textsubscript{OUT} = 5 V
**Figure 57.** Line Transient Response, $C_{IN}, C_{OUT} = 1 \mu F$, $I_{LOAD} = 1 mA$, $V_{OUT} = 1.8 V$

**Figure 58.** Line Transient Response, $C_{IN}, C_{OUT} = 1 \mu F$, $I_{LOAD} = 1 mA$, $V_{OUT} = 3.3 V$

**Figure 59.** Line Transient Response, $C_{IN}, C_{OUT} = 1 \mu F$, $I_{LOAD} = 1 mA$, $V_{OUT} = 5 V$
**THEORY OF OPERATION**

The ADP7102 is a low quiescent current, low dropout linear regulator that operates from 3.3 V to 20 V and provides up to 300 mA of output current. Drawing a low 750 μA of quiescent current (typical) at full load makes the ADP7102 ideal for battery operated portable equipment. Typical shutdown current consumption is 40 μA at room temperature.

Optimized for use with small 1 μF ceramic capacitors, the ADP7102 provides excellent transient performance.

Internally, the ADP7102 consists of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage.

If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

The ADP7102 is available in seven fixed output voltage options, ranging from 1.8 V to 9 V, and in an adjustable version with an output voltage that can be set to any voltage between 1.22 V and 19 V by an external voltage divider. The output voltage can be set according to the following equation:

\[ V_{OUT} = 1.22 \times (1 + \frac{R1}{R2}) \]

The value of R2 must be less than 200 kΩ to minimize errors in the output voltage caused by the ADJ pin input current. For example, when R1 and R2 each equal 200 kΩ, the output voltage is 2.44 V. The output voltage error introduced by the ADJ pin input current is 2 mV or 0.08%, assuming a typical ADJ pin input current of 10 nA at 25°C.

The ADP7102 uses the EN/UVLO pin to enable and disable the VOUT pin under normal operating conditions. When EN/UVLO is high, VOUT turns on; when EN is low, VOUT turns off. For automatic startup, EN/UVLO can be tied to VIN.

The ADP7102 incorporates reverse current protections circuitry that prevents current flow backwards through the pass element when the output voltage is greater than the input voltage. A comparator senses the difference between the input and output voltages. When the difference between the input voltage and output voltage exceeds 55 mV, the body of the PFET is switched to VOUT and turned off or opened. In other words, the gate is connected to VOUT.
**APPLICATIONS INFORMATION**

**CAPACITOR SELECTION**

**Output Capacitor**

The ADP7102 is designed for operation with small, space-saving ceramic capacitors but functions with most commonly used capacitors as long as care is taken with regard to the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 1 μF capacitance with an ESR of 0.2 Ω or less is recommended to ensure the stability of the ADP7102. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP7102 to large changes in load current. Figure 63 shows the transient responses for an output capacitance value of 1 μF.

![Figure 63. Output Transient Response, VOUT = 1.8 V, COUT = 1 μF](image)

**Input Bypass Capacitor**

Connecting a 1 μF capacitor from VIN to GND reduces the circuit sensitivity to PCB layout, especially when long input traces or high source impedance are encountered. If greater than 1 μF of output capacitance is required, the input capacitor should be increased to match it.

**Input and Output Capacitor Properties**

Any good quality ceramic capacitors can be used with the ADP7102, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V to 50 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

Figure 64 depicts the capacitance vs. voltage bias characteristic of an 0402, 1 μF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is ~ ±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

![Figure 64. Capacitance vs. Voltage Characteristic](image)

Use Equation 1 to determine the worst case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage.

\[
C_{\text{eff}} = C_{\text{bias}} \times (1 - \text{TEMPCO}) \times (1 - \text{TOL})
\]

where:

- \(C_{\text{bias}}\) is the effective capacitance at the operating voltage.
- TEMPCO is the worst case capacitor temperature coefficient.
- TOL is the worst case component tolerance.

In this example, the worst case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and \(C_{\text{bias}}\) is 0.94 μF at 1.8 V, as shown in Figure 64.

Substituting these values in Equation 1 yields

\[
C_{\text{eff}} = 0.94 \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.719 \mu F
\]

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP7102, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.
PROGRAMMABLE UNDervoltage LOckout (UVLO)

The ADP7102 uses the EN/UVLO pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 65, when a rising voltage on EN crosses the upper threshold, VOUT turns on. When a falling voltage on EN/UVLO crosses the lower threshold, VOUT turns off. The hysteresis of the EN/UVLO threshold is determined by the Thevenin equivalent resistance in series with the EN/UVLO pin.

The upper and lower thresholds are user programmable and can be set using two resistors. When the EN/UVLO pin voltage is below 1.22 V, the LDO is disabled. When the EN/UVLO pin voltage transitions above 1.22 V, the LDO is enabled and 10 μA hysteresis current is sourced out of the pin raising the voltage, thus providing threshold hysteresis. Typically, two external resistors program the minimum operational voltage for the LDO. The resistance values, R1 and R2 can be determined from:

\[ R1 = \frac{V_{\text{HYS}}}{10 \mu A} \]
\[ R2 = 1.22 V \times \frac{R1}{(V_{\text{IN}} - 1.22 V)} \]

where:

\( V_{\text{IN}} \) is the desired turn on voltage.

\( V_{\text{HYS}} \) is the desired EN/UVLO hysteresis level.

Hysteresis can also be achieved by connecting a resistor in series with EN/UVLO pin. For the example shown in Figure 66, the enable threshold is 2.44 V with a hysteresis of 1 V.

Figure 65 shows the typical hysteresis of the EN/UVLO pin. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The ADP7102 uses an internal soft start to limit the inrush current when the output is enabled. The start-up time for the 3.3 V option is approximately 580 μs from the time the EN active threshold is crossed to when the output reaches 90% of its final value. As shown in Figure 67, the start-up time is dependent on the output voltage setting.
POWER-GOOD FEATURE

The ADP7102 provides a power-good pin (PG) to indicate the status of the output. This open-drain output requires an external pull-up resistor to VOUT. If the device is in shutdown mode, current-limit mode, or thermal shutdown, or if it falls below 90% of the nominal output voltage, the power-good pin (PG) immediately transitions low. During soft start, the rising threshold of the power-good signal is 93.5% of the nominal output voltage.

The open-drain output is held low when the ADP7102 has sufficient input voltage to turn on the internal PG transistor. The PG transistor is terminated via a pull-up resistor to VOUT or VIN. Power-good accuracy is 93.5% of the nominal regulator output voltage when this voltage is rising, with a 90% trip point when this voltage is falling. Regulator input voltage brownouts or glitches trigger power no good signals if VOUT falls below 90%.

A normal power-down causes the power-good signal to go low when VOUT drops below 90%.

Figure 68 and Figure 69 show the typical power-good rising and falling threshold over temperature.

NOISE REDUCTION OF THE ADJUSTABLE ADP7102

The ultralow output noise of the fixed output ADP7102 is achieved by keeping the LDO error amplifier in unity gain and setting the reference voltage equal to the output voltage. This architecture does not work for an adjustable output voltage LDO. The adjustable output ADP7102 uses the more conventional architecture where the reference voltage is fixed and the error amplifier gain is a function of the output voltage. The disadvantage of the conventional LDO architecture is that the output voltage noise is proportional to the output voltage.

The adjustable LDO circuit may be modified slightly to reduce the output voltage noise to levels close to that of the fixed output ADP7102. The circuit shown in Figure 70 adds two additional components to the output voltage setting resistor divider. CNR and RNR are added in parallel with RFB1 to reduce the ac gain of the error amplifier. RNR is chosen to be equal to RFB2; this limits the ac gain of the error amplifier to approximately 6 dB. The actual gain is the parallel combination of RNR and RFB2, divided by RFB1. This ensures that the error amplifier always operates at greater than unity gain.

CNR is chosen by setting the reactance of CNR equal to RFB1 − RNR at a frequency between 50 Hz and 100 Hz. This sets the frequency where the ac gain of the error amplifier is 3 dB down from its dc gain.

\[
\text{RMS noise of the adjustable LDO without noise reduction} = 27.8 \mu\text{V rms}
\]

\[
\text{RMS noise of the adjustable LDO with noise reduction} = 19.95 \mu\text{V rms}
\]

Based on the component values shown in Figure 70, the ADP7102 has the following characteristics:

- DC gain of 4.09 (12.2 dB)
- 3 dB roll off frequency of 59 Hz
- High frequency ac gain of 1.76 (4.89 dB)
- Noise reduction factor of 1.33 (2.59 dB)
- RMS noise of the adjustable LDO without noise reduction of 27.8 \mu V rms
- RMS noise of the adjustable LDO with noise reduction (assuming 15 \mu V rms for fixed voltage option) of 19.95 \mu V rms
CURRENT LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP7102 is protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP7102 is designed to current limit when the output load reaches 400 mA (typical). When the output load exceeds 400 mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and/or high power dissipation) when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to zero. When the junction temperature drops below 135°C, the output is turned on again, and output current is restored to its operating value.

Consider the case where a hard short from VOUT to ground occurs. At first, the ADP7102 current limits, so that only 400 mA is conducted into the short. If self heating of the junction is great enough to cause its temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 135°C, the output turns on and conducts 400 mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 400 mA and 0 mA that continues as long as the short remains at the output.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so the junction temperature does not exceed 125°C.

THERMAL CONSIDERATIONS

In applications with low input to output voltage differential, the ADP7102 does not dissipate much heat. However, in applications with high ambient temperature and/or high input voltage, the heat dissipated in the package may become large enough that it causes the junction temperature of the die to exceed the maximum junction temperature of 125°C.

When the junction temperature exceeds 150°C, the converter enters thermal shutdown. It recovers only after the junction temperature has decreased below 135°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application is very important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 2.

To guarantee reliable operation, the junction temperature of the ADP7102 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air ($\theta_{JA}$). The $\theta_{JA}$ number is dependent on the package assembly compounds that are used and the amount of copper used to solder the package GND pins to the PCB.

Table 6 shows typical $\theta_{JA}$ values of the 8-lead SOIC and 8-lead LFCSP packages for various PCB copper sizes. Table 7 shows the typical $\Psi_{JB}$ values of the 8-lead SOIC and 8-lead LFCSP.

### Table 6. Typical $\theta_{JA}$ Values

<table>
<thead>
<tr>
<th>Copper Size (mm²)</th>
<th>LFCSP</th>
<th>SOIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>165.1</td>
<td>167.8</td>
</tr>
<tr>
<td>100</td>
<td>125.8</td>
<td>111</td>
</tr>
<tr>
<td>500</td>
<td>68.1</td>
<td>65.9</td>
</tr>
<tr>
<td>1000</td>
<td>56.4</td>
<td>56.1</td>
</tr>
<tr>
<td>6400</td>
<td>42.1</td>
<td>45.8</td>
</tr>
</tbody>
</table>

$^1$ Device soldered to minimum size pin traces.

### Table 7. Typical $\Psi_{JB}$ Values

<table>
<thead>
<tr>
<th>Model</th>
<th>$\Psi_{JB}$ (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LFCSP</td>
<td>15.1</td>
</tr>
<tr>
<td>SOIC</td>
<td>31.3</td>
</tr>
</tbody>
</table>

The junction temperature of the ADP7102 is calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA})$$  \hspace{1cm} (2)

where:

- $T_A$ is the ambient temperature.
- $P_D$ is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND})$$  \hspace{1cm} (3)

where:

- $I_{LOAD}$ is the load current.
- $I_{GND}$ is the ground current.
- $V_{IN}$ and $V_{OUT}$ are input and output voltages, respectively.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + [(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}$$  \hspace{1cm} (4)

As shown in Equation 4, for a given ambient temperature, input to output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure that the junction temperature does not rise above 125°C. Figure 71 to Figure 78 show junction temperature calculations for different ambient temperatures, power dissipation, and areas of PCB copper.
In the case where the board temperature is known, use the thermal characterization parameter, $\Psi_{JB}$, to estimate the junction temperature rise (see Figure 77 and Figure 78). Maximum junction temperature ($T_J$) is calculated from the board temperature ($T_B$) and power dissipation ($P_D$) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB})$$  \hspace{1cm} (5)$$

The typical value of $\Psi_{JB}$ is $15.1^\circ\text{C}/\text{W}$ for the 8-lead LFCSP package and $31.3^\circ\text{C}/\text{W}$ for the 8-lead SOIC package.

![Figure 77. LFCSP](image1.png)

![Figure 78. SOIC](image2.png)
**PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS**

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP7102. However, as listed in Table 6, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitor as close as possible to the VOUT and GND pins. Use of 0805 or 0603 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

![Figure 79. Example LFCSP PCB Layout](image1)

![Figure 80. Example SOIC PCB Layout](image2)
OUTLINE DIMENSIONS

COMPLIANT TO JEDEC STANDARDS MO-229-WEED-4

Figure 81. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-8-5)
Dimensions shown in millimeters

COMPLIANT TO JEDEC STANDARDS MS-012-AA

Figure 82. 8-Lead Standard Small Outline Package, with Exposed Pad [SOIC_N_EP]
Narrow Body
(RD-8-2)
Dimensions shown in millimeters
## ORDERING GUIDE

<table>
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<th>Model</th>
<th>Temperature Range</th>
<th>Output Voltage (V(^{1,3}))</th>
<th>Package Description</th>
<th>Package Option</th>
<th>Branding</th>
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<tbody>
<tr>
<td>ADP7102ACPZ-R7</td>
<td>−40°C to +125°C</td>
<td>Adjustable</td>
<td>8-Lead LFCSP_WD</td>
<td>CP-8-5</td>
<td>LHO</td>
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<td>RD-8-2</td>
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\(^1\) Z = RoHS Compliant Part.
\(^2\) For additional voltage options, contact a local Analog Devices, Inc., sales or distribution representative.
\(^3\) The ADP7102CP-EVALZ and ADP7102RD-EVALZ evaluation boards are preconfigured with a 3.3 V ADP7102