P(G)-VQFN Packages

PCB Assembly Recommendations

Solution Guide

Revision 1.2, 2015-05-07
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<tr>
<td></td>
<td>• Figure 4 updated to show the dimensions eA and eB.</td>
</tr>
<tr>
<td></td>
<td>• PG-VQFN-68 added to Table 2 Recommended PCB Pad Dimensions for VQFN Packages (all dimensions in mm).</td>
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Preface

This solution guide provides Printed Circuit Board (PCB) assembly recommendations for Lantiq’s P(G)-VQFN (Plastic (Green) Very Thin Profile Quad Flat Non Leaded) packages.

Organization of this Document

This document is organized as follows:

- Chapter 1, Package Description
- Chapter 2, Package Handling
- Chapter 3, Printed Circuit Board (PCB)
- Chapter 4, Board Assembly
- Chapter 5, Inspection
- Chapter 6, Rework
- Standards References
1 Package Description

The P(G)-VQFN (Plastic (Green) Very Thin Profile Quad Flat Non Leaded) package, as shown in Figure 1 and Figure 2, is a near chip-scale plastic encapsulated package. Array pads are provided on the package bottom and also an exposed die pad, which is typically soldered to the printed circuit board to achieve optimum electrical and thermal performance, and board level reliability. "G" denotes "green" VQFN packages, which means lead-free package materials (RoHS compliant) are used.

Features
- Optimized electrical performance
- Enhanced thermal performance with exposed die pad concept
- Leads and exposed die pad with solder plating
- Small footprint, thin package
- Package outline according to JEDEC MO220

![Figure 1 P(G)-VQFN with Punched Type Mold Compound](image1)

![Figure 2 P(G)-VQFN with Sawn Type Mold Compound](image2)
2  Package Handling

This chapter is organized as follows:

• Chapter 2.1, ESD Protective Measures
• Chapter 2.2, Packing of Components
• Chapter 2.3, Storage and Transportation Conditions

2.1  ESD Protective Measures

Semiconductor devices are normally electrostatic discharge sensitive devices (ESDS) requiring specific precautionary measures regarding handling and processing. An electrostatic charge may accidentally be discharged via an IC when it is touched by a person or processing tools. This can cause high current or voltage pulses which can damage or even destroy sensitive semiconductor structures. ICs may also be charged during processing. If the discharge takes place too quickly ("hard" discharge), it can cause load pulses and, worst case, electrical damage. Therefore ESD protective measures must ensure that there is no contact with charged objects and that the IC is not charged during processing. These measures cover the handling, processing and packing of ESDS devices. Recommendations regarding handling and processing are provided below.

2.1.1  Workplace ESD Protective Measures

• Standard marking of ESD protected areas
• Access controls, with wrist strap and footwear testers
• Air conditioning
• Dissipative and grounded floor
• Dissipative and grounded working and storage areas
• Dissipative chairs
• Ground bonding point for wrist strap
• Trolleys with dissipative surfaces and wheels
• Suitable shipping and storage containers
• No sources of electrostatic fields

2.1.2  Equipment for Personnel

• Dissipative/conductive footwear or heel straps
• Suitable smocks
• Wrist strap with safety resistor
• Volume conductive gloves or finger cots
• Regular training of staff

2.1.3  Production Installations and Processing Tools

• Machine and tool parts made of dissipative or metallic materials
• No materials with thin insulating layers for sliding tracks
• All parts reliably connected to ground potential
• No potential difference between individual machine and tool parts
• No sources of electrostatic fields

Detailed information on ESD protective measures may be obtained from the ESD Specialist via the Area Sales Offices. Our recommendations are based on the internationally applicable standards IEC 61340-5-1 and ANSI/ESD S2020.
2.2 Packing of Components

List of relevant standards that should be taken into consideration

Lantiq packs according to the IEC 60286-* series of standards:

- **IEC 60286-1** [1]
  Packaging of components for automatic handling –
  Part 1: Tape packaging of components with axial leads on continuous tapes

- **IEC 60286-2** [2]
  Packaging of components for automatic handling –
  Part 2: Packaging of components with unidirectional leads on continuous tapes

- **IEC 60286-3** [3]
  Packaging of components for automatic handling –
  Part 3: Packaging of surface mount components on continuous tapes

- **IEC 60286-4** [4]
  Packaging of components for automatic handling –
  Part 4: Stick magazines for electronic components encapsulated in packages of different forms

- **IEC 60286-5** [5]
  Packaging of components for automatic handling –
  Part 5: Matrix trays

- **IEC 60286-6** [6]
  Packaging of components for automatic handling –
  Part 6: Bulk case packaging for surface mounting components

Moisture Sensitive Surface Mount Devices

Lantiq packs according to:

- **IPC/JEDEC J-STD-033C** [7]
  Handling, packing, shipping and use of moisture/reflow sensitive surface mount devices

For the package body dimensions, refer to the detailed package outline drawings which can be requested from your Lantiq representative.

Other references

- **ANSI/EIA-481-D** [8]
  8 mm through 200 mm embossed carrier taping and 8 mm & 12 mm punched carrier taping of surface mount components for automatic handling

- **EIA-726** [9]
  8 mm punched & embossed carrier taping of surface mount components for automatic handling of devices generally smaller than 2.0 mm x 1.2 mm

- **EIA-747** [10]
  Adhesive backed punched plastic carrier taping of singulated bare die and other surface mount components for automatic handling of devices generally less than 1.0 mm thick

- **EIA/IS-763** [11]
  Bare die and chip scale packages taped in 8 mm & 12 mm carrier tape for automatic handling

- **EIA-783** [12]
  Guideline orientation standard for multi-connection package (design rules for tape and reel orientation)
2.3 Storage and Transportation Conditions

Improper transportation and unsuitable storage of components can lead to a number of problems during subsequent processing, such as poor solderability, delamination and package cracking effects.

List of relevant standards that should be taken into consideration:

- **IEC 60721-3-0 [13]**
  Classification of environmental conditions –
  Part 3: Classification of groups of environmental parameters and their severities –
  Introduction

- **IEC 60721-3-1 [14]**
  Classification of environmental conditions –
  Part 3 Classification of groups of environmental parameters and their severities –
  Section 1: Storage

- **IEC 60721-3-2 [15]**
  Classification of environmental conditions –
  Part 3: Classification of groups of environmental parameters and their severities –
  Section 2: Transportation

- **IEC 61760-2 [16]**
  Surface mounting technology –
  Part 2: Transportation and storage conditions of surface mounting devices (SMD) –
  Application guide

- **IEC 62258-3 [17]**
  Semiconductor die products –
  Part 3: Recommendations for good practice in handling, packing and storage

- **ISO 14644-1 [18]**
  Cleanrooms and associated controlled environments –
  Part 1: Classification of air cleanliness

### Table 1 Storage Conditions

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<th>Product</th>
<th>Storage Condition</th>
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<td>Wafer/die</td>
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<tr>
<td>Component - moisture sensitive</td>
<td>MBB (JEDEC J-STD-033*)</td>
</tr>
<tr>
<td>Component - not moisture sensitive</td>
<td>1K2 (IEC 60721-3-1)</td>
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</table>

¹) MBB = Moisture Barrier Bag

**Maximum Storage Time**

The conditions to be complied with in order to ensure problem-free processing of active and passive components are described in standard IEC 61760-2.

**Internet Links to Standards Institutes**

- American National Standards Institutes (ANSI)
- Electronics Industries Alliance (EIA)
- Association Connecting Electronics Industries (IPC)
- JEDEC Solid State Technology Association (JEDEC)
3 Printed Circuit Board (PCB)

This chapter is organized as follows:

- Chapter 3.1, General Remarks
- Chapter 3.2, PCB Pad Design
- Chapter 3.3, Solder Mask Layer
- Chapter 3.4, Vias in Thermal Pad
- Chapter 3.5, PCB Pad Finishes

3.1 General Remarks

The design and construction of a printed circuit board is a key factor in achieving high board assembly yields and sufficient reliability. Typical examples are the PCB pad designs for the perimeter lands and for the large central thermal pad, which is generally recommended to be soldered to the PCB to achieve optimum thermal, electrical and board level reliability performance. The via design and board finish also have to be taken into consideration. It should be emphasized that this document only provides general guidelines aimed at supporting customers in board design. Further optimization that takes into account the actual PCB manufacturer’s capability, the customer’s SMT process and product specific requirements must be carried out by the customer.

3.2 PCB Pad Design

Figure 3 shows a schematic cross section of a solder joint through a perimeter land. We recommend extending the PCB pad towards the package outside by approx. 0.25 mm compared to the package land. This is the value used to calculate the pad recommendations in Table 2. This extension of the PCB pad helps to develop a solder joint fillet along the side wall of the VQFN land. However, this cannot be guaranteed as this area is not plated. Further factors that influence the fillet formation are package exposure to the environment, the solder paste material and the reflow process. The forming of fillets is beneficial for solder joint reliability.

The detailed PCB pad values recommended in Table 2 for the various VQFN packages also assume a slight extension of the PCB pad towards the package center, in the range 0 - 0.05 mm. For VQFN packages with short distances between the lands and the thermal die pad, the value for the slight extension is kept to 0 to avoid the risk of solder bridging.

We recommend a pad width of 0.25 mm for pitch 0.5 mm, and 0.35 mm for pitch 0.65 mm.

The VQFN packages have a central die pad. The surface plating is the same as for the outer package pads. In most applications, the die pad allows a large quantity of heat to be transferred into the PCB to achieve higher thermal performance. Therefore, the pad should be soldered onto the “thermal” pad of the board. This also increases solder joint reliability and, for some applications/products, the electrical performance. We recommend using the die pad size on the VQFN package as the maximum “thermal” pad size on the PCB (see values in Table 2). A slightly smaller “thermal” pad is also possible.

![Figure 3: Schematic Cross Section of Perimeter Solder Joint](image-url)
Figure 4 shows a schematic drawing of the PCB metal design for perimeter pads and the thermal pad, and defines the important geometric parameters:

![Schematic drawing of PCB metal design](image.png)

Table 2 provides detailed information for the package specific dimensions depicted in Figure 4:

<table>
<thead>
<tr>
<th>Package Name</th>
<th>Package Size</th>
<th>VQFN Perimeter Land Size on Package</th>
<th>VQFN Die Pad Size</th>
<th>Perimeter Pad Size on PCB</th>
<th>Max. Size of Thermal Pad on PCB</th>
<th>Pad Gap</th>
<th>Pad Pitch</th>
<th>Pad Number (per side)</th>
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<td>11.1</td>
<td>0.40 27 27</td>
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</table>
3.3 Solder Mask Layer

Two basic types of solder pads are commonly used:

**Solder Mask Defined (SMD) Pad**

*Figure 5* shows the SMD pad. The copper metal pad is larger than the solder mask opening above it. Thus the pad area is defined by the opening in the solder mask.

![SMD Pad](image)

**Non Solder Mask Defined (NSMD) Pad**

*Figure 6* shows the NSMD pad. There is a solder mask clearance around each copper metal pad. The dimensions and tolerances of this clearance must ensure that the solder mask does not overlap the solder pad (dependent on the PCB manufacturer’s tolerances, 75 µm is a widely used value).

![NSMD Pad](image)

We recommend NSMD type solder pads for the perimeter solder pads, because the tolerances of the copper pads are lower than the solder masking process tolerances, and in order to create solder fillets along the solder pads of the board.

There should also be a ring of solder mask between the perimeter pads on the PCB and the thermal pad in the center in order to reduce the risk of solder bridging. If the distance between the perimeter pads and the metal of the thermal pad area is ≤ 300 µm, the solder mask should overlap the thermal pad metal area by ≥ 100 µm on each side.
3.4 Vias in Thermal Pad

Some products/applications require the “thermal” pad to be connected to inner copper layers of the PCB by vias. One reason may be to maximize the electrical performance, especially for products operating with high frequencies. Another reason may be the optimization of the thermal performance for products with high thermal power dissipation. In this case, plated through-hole vias, which are (if possible, fully) connected to inner and/or bottom copper planes of the board, help to distribute the heat into the board area. The heat penetrates from the chip over the package die pad and the solder joint to the thermal pad on the board.

A typical via hole diameter for such thermal vias is 0.3 mm. The number of vias in the thermal pad depends on the thermal requirements of the end product, the power consumption of the product, the application, and the construction of the printed circuit board. However an array of thermal vias with pitch 1.0 - 1.2 mm is a reasonable starting point for most products/applications, allowing for further optimization.

If the vias remain open while the board is being manufactured, solder may flow into the vias during VQFN board assembly (“solder wicking”). This could cause large voids in the “thermal” solder joint under the die pad, lower stand-off (which is controlled by the solder volume between the package die pad and the thermal pad on the PCB), and/or solder protruding from the other side of the board, which may disturb a second solder paste printing process on this other board side. If necessary, the solder wicking can be avoided by plugging the vias (filling with epoxy) or tenting the via with solder mask (for example, with a dry-film solder mask). Via tenting should be performed from the top as via tenting from the bottom gives rise to a significantly higher rate of voiding.

3.5 PCB Pad Finishes

The solder pads must have good wettability for the solder paste. All the finishes listed in Table 2 are well proven for SMT assembly. However, the quality of the plating/finish is even more important for fine pitch applications such as VQFN packages. Due to the uneven surface of the Hot Air Solder Leveling (HASL) finish, lead-free or lead containing HASL is less preferable for VQFN assembly (especially for pitch < 0.65 mm) compared to completely “flat” platings such as Cu-OSP (OSP: Organic Solderability Preservative), or electroless Sn or NiAu.

From the package point of view it is not possible to give a definite recommendation for the PCB pad finish. It also depends strongly on the board design, pad geometry, the components on the board and the process conditions.
4 Board Assembly

This chapter is organized as follows:

• Chapter 4.1, General Remarks
• Chapter 4.2, Solder Stencil
• Chapter 4.3, Solder Paste
• Chapter 4.4, Component Placement
• Chapter 4.5, Soldering
• Chapter 4.6, Cleaning

4.1 General Remarks

Many factors within the board assembly process influence the assembly yield and board level reliability, for example, the design and material of the stencil, the solder paste material, the solder paste printing process, component placement and the reflow process.

It should be emphasized that this document only provides general guidelines aimed at supporting customers in selecting the appropriate processes and materials. Further optimization that takes into account the actual PCB manufacturer’s capability, the customer’s SMT process and product specific requirements must be carried out by the customer.

Both P-VQFN with SnPb plating and lead-free PG-VQFN with Sn plating can be assembled with either SnPb based or lead-free SnAgCu based solder paste and reflow processes. If the plan is to assemble the P-VQFN package with SnPb plating and a lead-free soldering process, then special attention must be paid to ensure that the maximum specified temperature (on the moisture sensitivity caution label on the packing material) is not exceeded during processing (see also Chapter 4.5).

4.2 Solder Stencil

The solder paste is applied to the metal pads on the PCB by screen printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. In most cases, the thickness of the stencil has to be matched to the needs of all the components on the PCB.

A stencil thickness of 100 - 125 µm is recommended for VQFN packages of pitch up to 0.5 mm. A stencil thickness of 150 µm is also possible for VQFN packages of pitch 0.65 mm. If this does not meet the requirements of other packages on the same PCB, a step-down stencil should be considered. In order to ensure uniform, high solder paste transfer to the PCB, laser cut (mostly made from stainless steel) or electroformed stencils (nickel) are preferable. Rounding the corners of the apertures (radius ~50 µm) can aid good paste release.

The apertures for the perimeter solder joints should be of the same size as the metal pads on the PCB (for recommendations see Chapter 3). The stencil in the thermal pad area should be segmented into multiple smaller openings (see schematic example in Figure 7). One large opening would result in excessive solder volume under the VQFN die pad compared to the perimeter pads, and a significantly higher voiding rate and higher risk of solder balling.

In our tests we printed a total area of about 40 - 50% of the thermal pad with solder paste. This achieved good board assembly yield and reliability. The resulting solder joint stand-off was typically in the range 50 - 60 µm. The most appropriate way of segmenting depends on the number and location of vias (if existing) and the solder resist layout on the thermal pad. If the thermal via matrix is regular, the stencil openings should be arranged in areas between the vias. In our evaluations, we typically used opening sizes ranging from 0.4 mm² to 1.0 mm² depending on the via density and thermal pad size.
4.3 Solder Paste
Solder paste consists of a solder alloy combined with a flux system, with a typical volume split of 50% alloy and 50% flux. In terms of mass, this means approx. 90 wt% alloy and 10 wt% flux system. One of the functions of the flux system is to remove oxidation (contamination) from the surfaces to be soldered. The ability to remove contaminants is given by the activation level. A lead based solder paste metal alloy has to be of leaded eutectic or near-eutectic composition (SnPb or SnPbAg). A lead-free solder paste metal alloy composition (typically SnAgCu with Ag 3 - 4%, Cu 0.5 - 1%) can also be applied. A “no-clean” solder paste is preferable, because cleaning under the soldered VQFN may be difficult. The paste must be suitable for printing the solder stencil aperture dimensions. Type 3 paste is recommended. Solder paste is sensitive to storage time, temperature and humidity. Please adhere to the handling recommendations of the paste manufacturer.

4.4 Component Placement
Manual component positioning is not recommended as VQFN packages have to be placed very accurately. Component placement accuracies of ±50 µm are obtainable with modern automatic component placement machines using vision systems. These systems measure both the PCB and the components optically. The components are then placed on the PCB at their programmed positions. The fiducials on the PCB are either located at the edge of the PCB (for the entire PCB), or at individual mounting positions (local fiducials). They are detected by the vision system immediately before the mounting process. Package recognition is performed by a special vision system, which enables correct centering of the complete package.

The maximum tolerable displacement of the components is 20% of the metal pad width on the PCB (for non solder mask defined pads). Consequently for VQFN packages, the device pad to PCB pad misalignment must be better than 50 µm to ensure a sufficiently accurate mounting process. A wide range of placement systems can achieve this.

The following points are important:
- Especially on large boards, local fiducials close to the device can compensate for PCB inaccuracies.
- It is recommended that the ball recognition capabilities of the placement system are used, not the outline centering.
- To ensure that the packages are identified correctly by the vision system, adequate lighting and the correct choice of measuring modes are necessary. The accurate settings can be taken from the equipment manuals.
- If too much force is applied when a component is placed, solder paste may be squeezed out and cause solder joint shorts. On the other hand if too little force is applied, there may be insufficient contact between the package and the solder paste, which can lead to open solder joints or badly centered packages.
4.5 Soldering

To a large extent, the yield and quality of the assembly process are determined by the soldering. All the standard reflow soldering processes:

• Forced convection
• Vapor phase
• Infrared (with restrictions)

and typical temperature profiles are suitable for VQFN board assembly. However, wave soldering cannot be used. During the reflow process, the time each solder joint is exposed to temperatures above the solder liquidus temperature must be long enough to achieve the optimum solder joint quality, but overheating of the PCB and its components must be avoided. Please refer to the bar code label on the device packing for the peak package body temperature (on the “Moisture Sensitivity Caution Label” see also Chapter 4.5.2). It is important that the maximum temperature of the VQFN package during the reflow process does not exceed the specified peak temperature.

When using infrared ovens without convection, special care may be necessary to ensure a sufficiently homogeneous temperature profile for all the solder joints on the PCB, especially on large complex boards where the components, including those under the VQFN packages, have different thermal masses. The most recommended type of reflow process is forced convection reflow. A nitrogen atmosphere can improve solder joint quality, but is normally not necessary when soldering tin-lead metal alloys. In the case of the lead-free process with higher reflow temperatures, a nitrogen atmosphere may reduce oxidation and improve the solder joint quality.

The temperature profile of a reflow process is one of the most important factors in the soldering process. It is divided into several phases, each with a special function. Figure 8 shows the temperature profile for a forced convection reflow process used to solder P(G)-VQFN packages. Table 3 gives examples of the key parameters for such a solder profile, for both tin-lead and lead-free alloys. The individual parameters are influenced by various factors, not only by the package. It is essential to follow the solder paste manufacturer’s application notes.

In addition, most PCBs contain devices of more than one package type and, therefore, the reflow profile has to be matched to the requirements of all the components and materials. We recommend that the temperatures of the solder joints are measured using thermocouples beneath the respective packages. The fact that components with large thermal masses do not heat up at the same speed as lightweight components must be taken into account. The position and surroundings of the package on the PCB, as well as the PCB thickness can also influence the solder joint temperature significantly. It is also important to ensure that the maximum temperatures do not exceed Moisture Sensitivity Level (MSL) specifications (see Chapter 4.5.2).
The details given in Table 3 are examples, not recommendations (for reference only):

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Tin-lead Alloy (SnPb or SnPbAg)</th>
<th>Lead-free Alloy (SnAgCu)</th>
<th>Main Requirements From</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preheating rate</td>
<td>2.5 K/s</td>
<td>2.5 K/s</td>
<td>Flux system (solder paste)</td>
</tr>
<tr>
<td>Soaking temperature</td>
<td>140 - 170°C</td>
<td>140 - 170°C</td>
<td>Flux system (solder paste)</td>
</tr>
<tr>
<td>Soaking time</td>
<td>80 s</td>
<td>80 s</td>
<td>Flux system (solder paste)</td>
</tr>
<tr>
<td>Peak temperature</td>
<td>225°C</td>
<td>245°C</td>
<td>Alloy (solder paste)</td>
</tr>
<tr>
<td>Reflow time over liquidus</td>
<td>60 s</td>
<td>60 s</td>
<td>Alloy (solder paste)</td>
</tr>
<tr>
<td>Cool down rate</td>
<td>2.5 K/s</td>
<td>2.5 K/s</td>
<td>–</td>
</tr>
</tbody>
</table>

4.5.1 Double-Sided Assembly

VQFN packages are suitable for mounting on double-sided PCBs. In such cases, the PCB is assembled on one side first (including soldering) and then the other side is assembled.

4.5.2 Processing of Moisture-Sensitive Components

It is necessary to control the moisture content of components that are housed in moisture-sensitive packages such as the VQFN. The penetration of moisture into the package molding compound is generally caused by exposure to the ambient air. In many cases, moisture absorption leads to moisture concentrations in the component that are high enough to damage the package during the reflow process. Thus it is necessary to dry moisture-sensitive components, seal them in a moisture-resistant bag and only remove them immediately prior to mounting them on the PCB.
The time for which a component may remain outside the moisture-resistant bag (from opening the moisture-resistant bag until the final soldering process) is a measure of the sensitivity of the component to ambient humidity (Moisture Sensitivity Level, MSL). The most commonly applied standard IPC\textsuperscript{1)}/JEDEC J-STD-033\textsuperscript{*} defines eight different MSLs (see Table 4). Please refer to the "Moisture Sensitivity Caution Label" on the packing material, which provides information on the moisture sensitivity level of the product. It also specifies the maximum reflow temperature that must not be exceeded during board assembly by the customer.

Table 4 Moisture Sensitivity Levels (according to IPC/JEDEC J-STD-033\textsuperscript{*})

<table>
<thead>
<tr>
<th>Level</th>
<th>Floor Life (out of bag)</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Unlimited</td>
<td>≤30°C/85% RH</td>
</tr>
<tr>
<td>2</td>
<td>1 year</td>
<td>≤30°C/60% RH</td>
</tr>
<tr>
<td>2a</td>
<td>4 weeks</td>
<td>≤30°C/60% RH</td>
</tr>
<tr>
<td>3</td>
<td>168 hours</td>
<td>≤30°C/60% RH</td>
</tr>
<tr>
<td>4</td>
<td>72 hours</td>
<td>≤30°C/60% RH</td>
</tr>
<tr>
<td>5</td>
<td>48 hours</td>
<td>≤30°C/60% RH</td>
</tr>
<tr>
<td>5a</td>
<td>24 hours</td>
<td>≤30°C/60% RH</td>
</tr>
<tr>
<td>6</td>
<td>Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.</td>
<td>≤30°C/60% RH</td>
</tr>
</tbody>
</table>

If moisture-sensitive components have been exposed to the ambient air for longer than the time specified by their MSL, or the humidity indicator card indicates too much moisture when the package is opened, then the packages have to be baked prior to being assembled. Please refer to IPC/JEDEC J-STD-033\textsuperscript{*} for further details. Baking a package too often can lead to solderability problems due to oxidation and/or intermetallic growth. Please note that the packing material might not be able to withstand the baking temperature (see the labeling on the packing for the maximum allowed temperature).

4.6 Cleaning
Flux residue may be found around the solder joints after the reflow soldering process. If a "no-clean" solder paste has been used for the solder paste printing, the flux residue does not usually have to be removed after the soldering process.

Please note that it is difficult to clean beneath a VQFN package because of the small gap between the package and the PCB, and therefore it is not recommended. However if the solder joints have to be cleaned, the following points need to be taken into account when selecting the cleaning method and solution (for example, ultrasonic, spray or vapor cleaning):

- The type of the packages to be cleaned.
- The flux used in the solder paste (resin-based, water-soluble, etc.).
- Environmental and safety aspects.

Any cleaning solution residue should be removed/dried very thoroughly. Please contact the solder paste manufacturer for recommendations on which cleaning solutions to use.

\textsuperscript{1)} Association Connecting Electronics Industries (IPC)
Visual inspection of the solder joints using conventional AOI (automatic optical inspection) systems is limited to the outer surfaces of the joints. Since the non-wetting of the package lead side walls is not a reject criterion, the significance of an optical inspection is low.

Figure 9 Overview of a Soldered VQFN Package
Fused leads denote VQFN lands, which are directly connected to the die pad via the lead frame. As shown in Figure 10 and Figure 11, non or incomplete wetting of the lead side walls is not a reject criteria.

Figure 10 Non-Wetting of the Lead Side Walls is Not a Reject Criteria
The only reasonable method of realizing efficient inline control is the implementation of AXI (automatic X-ray inspection) systems. These are available as 2D and 3D solutions and usually consist of an X-ray camera and the hardware and software required for inspection, control, analysis and data transfer. AXI systems offer the user a fairly reliable way of detecting soldering defects such as poor soldering, bridging, voiding and missing parts. Please refer to the IPC-A-610C standard for further details on the acceptability of such electronic systems.

**Figure 11** Incomplete Wetting of the Lead Side Walls is Not a Reject Criteria

The cross-sectioning of a soldered package (**Figure 13**) or dye penetrant analysis can only be used for sample monitoring, as both of these methods destroy the device.
Special Notes for Lead-Free Solder Joints

Lead-free solder joints look different to tin-lead (SnPb) solder joints, which typically have a bright and shiny surface. Lead-free (SnAgCu) solder joints are often dull and grainy rather than shiny. These surface properties are caused by the irregular solidification of the solder, as the solder alloys used are not exactly eutectic (for example, the 63Sn37Pb solder alloy). This means that SnAgCu solders do not have a single melting point, but a melting range of several degrees.

Although lead-free solder joints have a dull surface, this does not mean that they are of lower quality or are weaker than the SnPb joints. Therefore, it is important to train inspection staff to recognise these new lead-free joints correctly, and/or to adjust optical inspection systems accordingly.
Rework

6 Rework

This chapter is organized as follows:

• Chapter 6.1, Tooling
• Chapter 6.2, Device Removal
• Chapter 6.3, Site Redressing
• Chapter 6.4, Reassembly and Reflow

If a defect component is found after board assembly, the device can be removed and replaced with a new one. It is not possible to repair individual solder joints on a component.

6.1 Tooling

The rework process is commonly performed using special rework equipment. Numerous systems are available on the market, however, the equipment should fulfill the following requirements if used to process these packages:

Heating

Hot air heat transfer to the package and PCB is highly recommended. The temperature and air flow used to heat the device is controlled. Programmable temperature profiles can be used to adapt to different package sizes and masses (for example, using a PC controller).

The preheating of the PCB from the underside is recommended. In particular, infrared heating can be used for this, but it should only support the hot air flow from the top side. Nitrogen can also be used instead of air.

Vision System

The bottom surface of the package, as well as the site on the PCB are observable. A split vision optic is implemented to superimpose the component and board images. This enables precise alignment of the package with the PCB. The microscope magnification and resolution are appropriate for the pitch of the device.

Moving and Additional Tools

The tool is able to move across the whole area of the PCB. The recommended placement accuracy is better than ±100 μm. The system is able to remove solder residue from the PCB pads (special vacuum tools).

6.2 Device Removal

If a defect component is to be sent back to the supplier, it must be ensured that no further defects are introduced when removing the component as this would interfere with failure analysis to be carried out by the supplier. This includes the following recommendations:

Moisture

Depending on the moisture sensitivity level, the package may have to be dried before removal. If the maximum storage time out of the moisture-resistant bag (see label on packing material) is exceeded after board assembly, the PCB must be dried according to the recommendations (see Chapter 4.5.2), otherwise too much moisture may have accumulated and damage may have occurred (popcorn effect).

Temperature Profile

During the soldering process, it should be ensured that the package peak temperature is not higher nor the temperature ramps steeper than for the standard assembly reflow process (see Chapter 4.5).
Mechanics
Do not apply excessive mechanical force to remove the device, otherwise failure analysis of the package may be impossible or the PCB might be damaged. Pipettes can be used for large packages (implemented in most rework systems), whereas tweezers may be more practical for small packages.

6.3 Site Redressing
After the defect component has been removed, the pads on the PCB have to be cleaned of solder residue. Do not use steel brushes as steel residue can lead to poor solder joints. Before placing a new component on the PCB, it is recommended that solder paste is applied to each PCB pad by printing (special micro stencil) or dispensing. It is recommended that only no-clean solder paste is used.

6.4 Reassembly and Reflow
After the site has been prepared, the new package can be placed on the PCB. It is positioned exactly above the PCB pads, just high enough to ensure that there is no contact between the package and the PCB. The package is then dropped into the printed or dispensed flux or solder paste deposit (zero-force-placement). During the soldering process, it should be ensured that the package peak temperature is not higher nor the temperature ramps steeper than for the standard assembly reflow process (see Chapter 4.5).
Standards References

   Packaging of components for automatic handling –
   Part 1: Tape packaging of components with axial leads on continuous tapes

   Packaging of components for automatic handling –
   Part 2: Packaging of components with unidirectional leads on continuous tapes

   Packaging of components for automatic handling –
   Part 3: Packaging of surface mount components on continuous tapes

   Packaging of components for automatic handling –
   Part 4: Stick magazines for electronic components encapsulated in packages of different forms

   Packaging of components for automatic handling –
   Part 5: Matrix trays

   Packaging of components for automatic handling –
   Part 6: Bulk case packaging for surface mounting components

   Handling, packing, shipping and use of moisture/reflow sensitive surface mount devices

   8 mm through 200 mm embossed carrier taping and 8 mm & 12 mm punched carrier taping of surface mount components for automatic handling

[9] EIA/ECA-726 Edition 02
   8 mm punched & embossed carrier taping of surface mount components for automatic handling of devices generally smaller than 2.0 mm x 1.2 mm

    Adhesive backed punched plastic carrier taping of singulated bare die and other surface mount components for automatic handling of devices generally less than 1.0 mm thick

    Bare die and chip scale packages taped in 8 mm & 12 mm carrier tape for automatic handling

    Guideline orientation standard for multi-connection package (design rules for tape and reel orientation)

    Classification of environmental conditions –
    Part 3: Classification of groups of environmental parameters and their severities –
    Introduction

[14] IEC 60721-3-1 Edition 2.0 1997-02
    Classification of environmental conditions –
    Part 3 Classification of groups of environmental parameters and their severities –
    Section 1: Storage

    Classification of environmental conditions –
Part 3: Classification of groups of environmental parameters and their severities –
Section 2: Transportation

   Surface mounting technology –
   Part 2: Transportation and storage conditions of surface mounting devices (SMD) –
   Application guide

   Semiconductor die products –
   Part 3: Recommendations for good practice in handling, packing and storage

[18] ISO 14644-1:1999
   Cleanrooms and associated controlled environments –
   Part 1: Classification of air cleanliness