The Movement to Large Array Packaging: Opportunities and Options

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Mobile Products Continue to Get Thinner

Source: ASE.
Smartphone ASPs Continue to Decline

- Smartphone ASPs continue to decline
- Creates price pressure on packages

Source: Adapted from IDC
What Packaging Solutions Enable Thin Products? And How Do We Lower Cost?

- Wafer Level Package?
- FO-WLP (reconstituted wafer)?
- Embedded die solution?
iPhone Trends: Increasing Number of WLPs

Shown to scale

Source: TechSearch International, Inc., adapted from TPSS.
Drivers for WLP

- Major applications for WLP:
  - Smartphones (highest volume application)
  - Digital cameras and camcorders
  - Laptops and tablets
  - Medical
  - Automotive
  - Wearable electronics such as watch

- WLP meets system packaging needs
  - Small form factor
  - Need for low profile packages
  - Lower cost (less material)

- Form Factor is Key
  - Low profile
  - Limited space on PCB
Conventional WLP Applications

- Conventional WLPs for many device types (analog, digital, sensor, discrete)
  - Power management IC
  - Audio CODEC
  - RF
  - IPD, ESD protection, filter
  - LED driver
  - Electronic compass
  - Controller
  - MOSFET
  - Image sensors
  - Ambient light sensors
- Conventional WLPs trends
  - Highest I/O count 309 (Fujitsu power management IC)
  - Largest body size Apple/Cirrus Logic Audio CODEC 5.72 x 6.03 x 0.59 mm, 121 solder balls, 0.5mm pitch
  - Increasing number of 0.4mm pitch parts, some 0.35mm pitch
  - Fine pitch parts need high-density PCB to route signals

Source: ASE.
What Set the Stage for FO-WLP?

• Historically, conventional WLPs for low I/O small die
  – 2 to 100 I/Os
  – Next 100s of I/Os
  – Now 400+ I/Os

• With increased I/O can’t “fan-in” using conventional WLP

• Need for split die package or multi-die package

Source: Casio Micronics

Source: ASE

Intel Wireless Division
LTE analog baseband
5.32 x 5.04 x 0.7mm eWLB
127 balls, 0.4mm pitch
FO-WLP Drivers

- Smaller form factor, lower profile package: similar to conventional WLP in profile (can be ≤0.4 mm)
- Thinner than flip chip package (no substrate)
- Support increased I/O density
- Excellent electrical and thermal performance
- Excellent high temperature warpage performance
- Fine L/S (10/10µm)
- Can enable a low-profile PoP solution as large as 15 mm x 15 mm
- Multiple die in package possible
- Die fabricated from different technology nodes can be assembled in a single package

Source: STATS ChipPAC.
Multi-Die FO-WLP Solution

- 2 Layer-RDL Interconnection
- 2 Active Die + 10 Passives 0201 SMD

Source: NANIUM
Device types include RF such as Bluetooth, NFC, GPS, PMIC, automotive radar, future application processors

Assumes that cost targets, business, and reliability requirements are met
FO-WLP Merchant Suppliers Status

- Amkor Technology redeploying FO-WLP with new 300mm line (eWLB) in K4 plant
- ADL Engineering 200mm pilot line in Taiwan
- ASE license for Infineon’s eWLB with 300mm in Taiwan, also offers “chip last” panel version
- Deca Technologies (300mm “panel” format)
- FCI/Fujikura (embedded WLP in flex circuit)
- NANIUM (300mm wafer) license for Infineon’s eWLB
- NEPES (300mm line in Korea)
- SPIL (300mm wafer, R&D on panel)
- STATS ChipPAC (300mm wafer) will be purchased by JCET, license for Infineon’s eWLB
- TSMC (300mm wafer InFO WLP)
- New supplier TBD
What’s Next?.....
Wafer Processing Moves Closer to PCB Fabrication
Panel Level is: The intelligent combination of Wafer Level Processing and PCB Processing (Fraunhofer IZM in Germany)

“Fusion” of semi WLP / LCD / PCB / Solar / flexible electronic infrastructures

• Finer lines and spaces in combination with semiconductor equipment and organic substrates
• Embedding of bare dies into organic substrates
• Glas, PCB, Filled Epoxy
PLP Strategies

Panel-Size FO-WLP

- Large-area molding 18" x 24"
- Through mold vias for 3D
- Interconnects using PCB materials & technology
- Mold embedding of sensors

PCB Embedding

- Use of new polymers / laminates
  - thin layers (10 µm) for high density
  - high breakthrough (>40 kV/mm) for power
- Improved resolution for interconnects
  10 µm → 5 µm → 2 µm
- Processes to reduce warpage

Source: Fraunhofer IZM.
PCB Embedding Today: Power and Logic

The production of embedded packages increasing

Smart Phone Market
- DC/DC converters
- Power management units
- Connectivity module

Computer market
- MOSFET packages
- Driver MOS SiPs

PCB Embedding Technology is implemented or will come soon at
- PCB manufacturers
- Semiconductor manufacturers
- OSATs

Source: Fraunhofer IZM.
Fraunhofer IZM Substrate Integration Line

**Placement**
- Datacon evo/ASM Siplace CA3

**Accuracy**
- Mahr OMS 600/IMPEX proX3

**Molding**
- WL: Towa up to 8"
- PL: APIC up to 18”x24” incl. 12” WL (Q3 – 2014)

**Lamination**
- Lauffer/Bürkle

**Laser Drilling**
- Siemens Microbeam/Schmoll Picodrill with HYPER RAPID 50

**Mech. Drilling**
- Schmoll MX1

**Cu Plating**
- Ramgraber automatic plating line

**Imaging**
- Orbotech Paragon Ultra 200

**Etching**
- Schmid
Panel Molding 18”x 24” – APIC Yamada

Equipment in Japan before shipment

Large area compression molding:
- Wafer Level: 300 mm up to 450 mm possible
- Panel Level: 18” x 24” (456 x 610 mm²)
- Lamination

Up and Running as of Q4/2014

First molded panel 18” x 24”
Amkor/J-Devices Panel Level Processing

- Starts with copper base plate (provides good thermal performance)
- Build substrate on top of die, ball attach, and singulation

Source: J-Devices.
FCI’s ChipletT Fan-Out on Flex Circuit

Wafer Level Packaging Process
- Forming RDL
- Backgrinding / Polishing
- Singulation

Flexible Printed Circuit Process
- Forming Copper Circuitry
- Opening Via Holes
- Proprietary Via Fill Technology

Co-Lamination
- Die Embedding, Layer Stack Up & Lamination

Backend Processing
- SMT, Molding, Bumping, Marking, Singulation

Source: FlipChip International.
Chipset™ Embedded Die Panel Processing

- Panel Scale Embedding Process
- Precision Embedded Component Placement
- Single Step Lamination
- Current Panel Size: 250 mm x 350 mm
- Panel Size Extendibility to 350 mm x 500 mm

Source: FlipChip International, Inc.
ASE’s Fan Out Chip Last Package

- Utilizing Low Cost FC Coreless Substrate
  - Embedded Traces & Pads
  - Fine Pitch capable

- Combined with Mass Reflow fine pitch Cu Pillar FC & Molded Underfill (MUF)

- Creates new Paradigm in low cost Fan out Packaging
  - Low Cost Coreless Substrate
  - Chip Last vs Chip First for Higher Assembly yields
  - Fine Pitch bumping direct on die pad without RDL
  - Thicker Copper (15-50 µm) allows higher current
  - Thin Package < 375µm
  - MSL 1

Source: ASE.
FO-WLP Panel Issues (≥17mm x 17mm)

• What size panel is feasible?
• Assembly of die on panel
  – Die placement accuracy may be more difficult to control with large panels
  – Large area bonders may be required
  – Throughput (time required to pick and place die in panel)
  – How is placement accuracy impacted by tape and mold compound?
  – What level of inspection is required to verify accuracy? What speed?
• Dielectric dispense methods?
  – Spin coat? Other methods?
  – How to control run-out at edge?
  – Need inspection for even coating?
• Molding materials and process?
• Panel warpage
  – Warpage increases with panel size
  – Impact of materials (mold compound and filler)
  – What type of inspection is requires and how will it work with warped panels
• Via formation method (minimum via diameter)
  – Via alignment
• Metal plating
  – Metal to dielectric interface (what inspection requirements?)
  – How to sputter seed layer?
• Interconnect reliability? Inspection for broken metal traces etc.
• Singulation method?
• Solder ball placement and inspection method?
Conclusions

- Mobile produces require low profile packages
  - Fan-in WLP
  - FO-WLP
  - Embedded die
- Declining ASPs for end products create price pressure driving development of new low cost package options
- Demand for lower cost solutions drives adoption of large area packaging
  - Panel-based processing
- Adoption of new panel technology means the wafer fab side, back end assembly, and PCB segments are merging
  - Challenges in panel level processing create opportunities for all
Thank you!

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