EUV lithography: On the move from pre-production to production
Eric Hendrickx, imec
Co-authors – imec EUV team

- Mieke Goethals
- Danilo De Simone
- Philippe Foubert
- Ivan Pollentier
- Rik Jonckheere
- Bart Baudemprez
- Emily Gallagher
- Vicky Philipsen
- Lieve Van Look
- Jan Hermans
- Geert Vandenberghe
- Kurt Ronse
- Greg McIntyre
Contents

Imec EUV program
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– EUV reticles
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Advanced litho program
Mission statement 2014-2016

• Explore, develop and verify the most promising patterning solutions for N10, N7, N5....

  – Directed Self-Assembly (DSA) program line
    • Optimization of the DSA process mainly to reduce defectivity
    • Demonstrate integration of a DSA flow in a next generation critical level
  
  – EUV Lithography (EUVL) program line
    • EUV resist screening, process optimization (N7 main focus)
    • EUV reticles – defect contribution understanding, mitigation and reduction
    • EUV scanner\source characterization, providing stable and reliable cluster to the customer
    • EUV extendibility to N5 and beyond – reticle implications, resist implications, CoO

  – Scaling and patterning program line
    • Explore various patterning solutions for various layout styles for printability
    • Verify selected set of patterning solutions in Si
<table>
<thead>
<tr>
<th>2006 - 2011</th>
<th>2011 - now</th>
<th>Installing now</th>
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</thead>
<tbody>
<tr>
<td>ASML Alpha-Demo tool</td>
<td>ASML NXE:3100 pre production</td>
<td>ASML NXE:3300 production</td>
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<tr>
<td>LS: 40nm → 27nm</td>
<td>LS: 27nm → 22nm</td>
<td>LS: 22nm → 13nm</td>
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<tr>
<td>0.25 NA</td>
<td>0.25 NA</td>
<td>0.33 NA</td>
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Improvements in Resists, masks, CD control, overlay, ...
NXE:3100

• Main specifications

– Field size: 26x33mm²
– NA=0.25 and σ=0.81
– 6 off-axis illumination conditions
– Flare < 8%
– MMO vs NXT:1950i < 7nm

Interfaced to TEL LITHIUS™ Pro for EUV

SUSS MicroTec
MaskTrack Pro

EUV Technologies
Outgassing tool
EUV Chemically amplified resists
Current main problem

- At resolution limit, defect mechanism no 1 is pattern collapse
- None of the resists come close to the required LWR at an acceptable sensitivity

Strong need for alternative EUV resists / materials

- Investigating CAR enablement – new inorganic resists
  - Rinse methods optimization
  - Dry development rinse process
  - Negative tone imaging
  - Metal containing resists

- Screening chemically amplified resists continues
  - As benchmark
  - To cover short term needs (alternative materials typically less mature)
Preparing for <20nm LS on 33x0
Continued CAR Resistscreening on NXE:3100

**LS resists** are not meeting <4nm LWR 3s and use higher dose to resolve 18nm LS – resolution is collapse limited – sensitive to rinse

**CH resists** – not meeting <1nm LCDU spec at 24nm dense

Fundamental improvements are needed
Preparing for <20nm LS on 33x0
CAR ultimate resolution at 0.33 NA

small sample screening – DIPOLE 45 – 30nm FT

<table>
<thead>
<tr>
<th>L18P36</th>
<th>L17P34</th>
<th>L16P32</th>
<th>L15P30</th>
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<tbody>
<tr>
<td>32mJ</td>
<td>31mJ</td>
<td>29mJ</td>
<td></td>
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<tr>
<td>18.22nm</td>
<td>16.89nm</td>
<td>16.8nm</td>
<td></td>
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<tr>
<td>LER 3.1 nm</td>
<td>LER 3.1 nm</td>
<td>LER 3.3nm</td>
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Ultimate resolution is 16 nm HP - 3.3nm LER with DtS of 29 mJ/cm²
Strong Line collapse occurs at 15nm HP
Alternative materials - Preventing line collapse

Dry Development Rinse process concept

Strengths: Line collapse reduction, etch resistance improvement

Peculiarity: reversed patterning process

NISSAN CHEMICAL INDUSTRIES, LTD.
Alternative materials - Preventing line collapse

Dry Development Rinse process demonstration

19nm LS, traditional develop - Resist prone to collapse

19nm LS, Nissan Dry Development Rinse Process – less collapse

First demonstration of pattern collapse reduction through DDRM
Why NTD in EUV?

Currently **Negative Tone imaging** process is **largely used on the industry on 193i tools** with large benefits in process window if compared to Positive Tone process.

- NTD was not tested yet in EUV – now tests are ongoing.
**NTD vs. PTD**

22 nm HP EUV RESIST LS PERFORMANCE

Currently Sensitivity and LER of NTD and PTD materials are in the same range
EUV Masks
Current main focus is on defectivity

- Can we make defect free masks?
  - Embedded defects in multilayer mirror occur, but are difficult to detect and mitigate

- Can we keep the EUV mask clean?
  - Correct mask handling, with zero added particles in scanner
  - Mask cleaning solution that permits frequent mask cleaning
Can we make defect free EUV masks?

- Embedded ML mask defectivity still is high (EUVL2013 – factor 10)
- Actinic blank inspection tools are under development (EIDEC/Lasertec ABI)
- Imec is collaborating with EIDEC to link ABI defectivity to NXE:3x00 wafer data
- After finding multilayer defect, mitigation is possible (shift under absorber, or absorber compensation repair)
Can we keep the EUV masks clean? Mask handling developed at imec

Mask shop

Mask cleaner MT-Pro

InSync: Automated transfer

BS inspection: on Nanometrics SPARK

FS and BS cleaning

Dedicated pod per mask

EUV Pod (‘A’ type shippable)

EUV Pod (‘A’ type inner pod)

Entegris storage cabinet

NXE:3100
3300 config.
Disto monitor
FS\BS defect monitor

Infrastructure and procedures developed to reduce particle adders on mask frontside and backside
Can we keep the EUV masks clean?
Low-impact mask cleaning solution

– Mask cleaning is required for small particles added to the frontside of the mask

– After optimizing mask cleaning recipe – demonstrated >100 cleans with no CD impact

– Performance of mask cleaning evaluated on reticles with etched ML for dark image border generation

• At field edge with etched ML – quantified cleaning impact as 5.6nm exposure field edge shift (4x) per clean (2 masks)
Can we keep the EUV masks clean?
Frontside particle adders in 3100 scanner

- Number of defects repeating from die-die on wafer, counts mask defects and particle adders on mask
- Mask cycling in scanner was done, to increase mask handling
- Increase of number of die-die repeating defects on wafer points to particle adder on mask
- By optimizing mask environment in 3100 scanner, a similar low chance for adding a particle is now demonstrated on 3100 as reported on 3300

R. Peeters et al
SPIE 2014
Outlook to NXE:3300

- NXE:3300 installation and preparation are ongoing
  - Anticipated throughput 30 wph in Feb 2015
  - Masks preparation
    - Monitormasks generated
    - OPC completed and executed for N10 device masks (3300 DEMO exposure)
    - First OPC model calibration ongoing towards N7 (3300 DEMO exposure)
Outlook to NXE:3300

22nm LS process of record test at 0.25NA

- NXE:3100 exposure
- TEL Lithius Pro
- Dipole 60-X illumination, 20.5 mJ/cm²
- Full wafer and full field exposure
- CD measured in 3 x 5 field positions, including field edges
- Raw data reported – no corrections applied
NXE:3300 first access results

N10 logic design printing verification after OPC

Resistscreening, 16nm LS process window

OPC model calibration wafer exposure for SN2 OPC model calibration

Models calibrated with rms <1.0nm
## Conclusions

<table>
<thead>
<tr>
<th>NXE:3100</th>
<th>Throughput</th>
<th>More than 9000 wafers exposed (3 years) Source collector mirror influences power level ~6 months collector mirror lifetime</th>
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<tbody>
<tr>
<td></td>
<td>Resists</td>
<td>CAR at limits – sensitive to developer conditions and pattern collapse Alternative techniques sometimes promising, but also not yet mature</td>
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<tr>
<td></td>
<td>Masks</td>
<td>ML embedded defects still challenging Good progress in mask FS particle adders Mask backside particles can be controlled</td>
</tr>
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<table>
<thead>
<tr>
<th>NXE:3300</th>
<th>Throughput</th>
<th>Expect 30 wph in Q1 2015</th>
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<tbody>
<tr>
<td></td>
<td>Process</td>
<td>TEL Lithius Pro-Z track ready, resists selected</td>
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<tr>
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<td>Mask</td>
<td>First OPC model calibration, mask fabrication exercises completed – N10 masks available</td>
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