Guidelines for Printed Circuit Board Assembly (PCBA) of UTAC Group’s Grid Array Package (GQFN) and its Board Level Reliability

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Overview

- Introduction
  - GQFN process flow
- GQFN Package Characterization
  - Thermal performance
  - Electrical performance
- GQFN’s PCB Assembly guidelines & BLR
  - PCBA guidelines
  - Temperature cycling on board
  - Drop test
- Conclusion
Introduction

- UTAC’s next generation Grid Array QFN (GQFN) provide highest I/O density among lead frame based package technology
- GQFN’s routable technology offers cost effective devices in the smallest possible footprint
- GQFN enables design freedom
  - Stacked die
  - Multi-chip
  - Passive component
  - Flip chip/ wirebond
- Feasible conversion of 2-layer laminate BGA and delivers MSL-1
UTAC Quad Flat no Lead Packages

QFN
QFN Fine Pitch 0.4/0.35/0.3
LLGA
Dual Row QFN
TLA
HLA
GQFN


Increasing I/O or Miniaturization
HLA vs GQFN Process Flow

1. Metal Frame
2. Partial Etch
3. Selective Plating
4. Die attach and wire bond
5. Mold encapsulation
6. Etch back Process
7. Soldermask
   - Ball Mount (Optional)
   - Package Singulation

7. Insulation Mold
   - Ball Mount (Optional)
   - Package Singulation
GQFN Process Flow

Top View: Single unit on bare leadframe from supplier

PPF Plating

Cu Base

Cu Trace

Screen print on Die back and D/A on leadframe

Die

Wirebond

Bondwire

Mold

1st Mold

X-Ray View (Showing top & Bottom)

Actual Terminal Plating

Bottom View: Single unit on bare leadframe from supplier

Bottom View after 1st mold

Etching Process

Copper Etched out

2nd Mold
Insulation mold

- Insulation Mold process poses risk in terms of mold filling ability because of tight clearance in bottom half etch leadframe and customizable irregular shaped I/Os.

- Process, design and materials optimization and potential risks were mitigated:
  - Mold flow simulation
  - Mold tooling design
  - Film assist molding
  - Process parameters, transfer profile and pressure
  - Mold material properties and fine filler technology

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<thead>
<tr>
<th></th>
<th>10% fill</th>
<th>50% fill</th>
<th>90% fill</th>
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Package characterization

- With routable traces and array I/Os, it is feasible to convert organic substrate base package to GQFN
  - better reliability(MSL-1) and lower cost

- Preconditioning (J-STD-20D.1) MSL-1, 168hrs, 85°C/85% RH
- Temp Cycle (JESD22-A104, Cond. C (-65 to 150°C), 1,000 cycles
- High Temp. Storage (JESD22-103 & A113) 150°C, 1,000 Hrs
- Unbiased Temp./Humidity (JESD-22A118) 130°C/85% RH 192 Hrs
The Computational Fluid Dynamics (CFD) simulation study

- Identical power dissipation, die size, die thickness and test environment
- Differences in package structure
  - FBGA model: 2-layers substrate with vias
  - GQFN model: routable leadframe

<table>
<thead>
<tr>
<th>1. Package size (mm)</th>
<th>FBGA: 5.0 x 5.0 x 0.53</th>
<th>GQFN: 5.0 x 5.0 x 0.45</th>
</tr>
</thead>
<tbody>
<tr>
<td>2. Die size (mm)</td>
<td>2.9 x 2.65 x 0.1</td>
<td></td>
</tr>
<tr>
<td>3. Substrate/Leadframe thickness (mm)</td>
<td>0.13 (2L) 0.015mm trace</td>
<td>0.1mm</td>
</tr>
<tr>
<td>4. PCB: JEDEC 2S2P (4L) , 1S0P (2L) board as per JESD 51-7 and JESD 51-3</td>
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</table>
Thermal Test Set Up

JEDEC Still Air Chamber

$\theta_{JA}$ - Junction to ambient

JEDEC Forced Air Chamber

$\theta_{JMA}$ - Junction to moving air

JEDEC PCB

Ambient 25°C

Ring cold plate

$T_l$

$T_b$

Top cold plate

$\theta_{JC}$ - Junction to case

Top Cold Plate

Ring Cold Plate

$\theta_{JB}$ - Junction to board

JEDEC PCB

Insulation

Insulation

Air Flow

1-3m/s
Thermal Performance

- GQFN has superior thermal capability in all aspects

FBGA Max temp: 55.7°C at 0.5W

GQFN Max temp: 51.85°C at 0.5W

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Air flow</th>
<th>FBGA 5x5mm (°C/W)</th>
<th>GQFN 5x5mm (°C/W)</th>
<th>% improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Theta JA</td>
<td>0</td>
<td>61.4</td>
<td>53.7</td>
<td>12.5%</td>
</tr>
<tr>
<td>Theta JMA</td>
<td>1</td>
<td>52.6</td>
<td>46.2</td>
<td>12.2%</td>
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<tr>
<td>(moving air)</td>
<td>2</td>
<td>51.0</td>
<td>44.7</td>
<td>12.4%</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>49.9</td>
<td>43.7</td>
<td>12.4%</td>
</tr>
<tr>
<td>Theta JB</td>
<td>0</td>
<td>32.0</td>
<td>24.1</td>
<td>24.7%</td>
</tr>
<tr>
<td>Theta JC</td>
<td>0</td>
<td>11.7</td>
<td>10.7</td>
<td>8.5%</td>
</tr>
</tbody>
</table>
Electrical Simulation Model

- Both packages were simulated using ADS (Advance Design System)

### Table

<table>
<thead>
<tr>
<th>Item</th>
<th>FBGA 5x5mm</th>
<th>GQFN 5x5mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate/ Leadframe Thickness (mm)</td>
<td>0.13</td>
<td>0.1</td>
</tr>
<tr>
<td>Wire Type/ Loop height</td>
<td>25um Au/ 0.1mm</td>
<td></td>
</tr>
<tr>
<td>Solder Ball (mm)</td>
<td>0.17</td>
<td>0.1</td>
</tr>
</tbody>
</table>
Electrical Performance - S-Parameter

- Scattering parameter analysis for high frequency application in GHz range
- A frequency sweep from DC to 30GHz on the longest span of the signal for each package
- The GQFN package will have a good electrical performance up to 3.9GHz that is 1GHz higher than FBGA package which is limited at 2.85GHz
Package miniaturization

- GQFN offers smaller form factor and package bottom termination by engaging routing technology with multi-row or full grid array pad layout
- Flexible to organize critical electrical paths for optimum parasitic values

10x10 mm QFP 64L (Footprint 12x12mm)  
9x9 mm QFN 64L (Footprint 9x9mm)  
5x5 mm GQFN 64L (Footprint 5x5mm)

![Diagram of package miniaturization with inductance and capacitance values](chart.png)
PCB Assembly guidelines

- Thermal vias recommended on the PCB thermal pad to boost thermal performance
  - Filled or plugged vias desirable
  - Vias quantity depends on the package power dissipation
- The PCB land pattern match with GQFN terminal and exposed pad
  - Soldering exposed pad reduces stress and enhanced direct thermal path
- PCB terminal approximately a 1:1 ratio with the package lead
  - Variation in PCB pad size is possible depends on requirement
PCB Assembly guidelines

- Stainless steel *stencils* with thickness of 0.075mm – 0.127mm (3 – 5 mils) are recommended
  - Opening 1:1 with pad size; smaller aperture size optional
  - Fine tune thickness and opening for optimal solder volume
- No clean *solder paste* is preferred for low standoff and tight openings
  - Type 4 solder for fine pitch
PCB Assembly guidelines

- GQFN packages can be very small with fine terminal pitch
  - +/-0.050mm package placement tolerance
  - Low placement pressure to prevent paste smearing or squeezing out

- Convection mass *reflow* techniques as part of standard SMT process
  - Profile should follow the solder paste supplier’s recommendation
    - *Pb-free solder*, peak temp. <260°C, time above liquidus temperature (217°C) of 45 seconds
    - *Eutectic solder*, peak temp. <240°C, time above liquidus temperature (183°C) of 45 seconds
PCB Assembly guidelines

- GQFN rework processes are very similar to or simplification of ball grid array package’s rework processes
  - Board preheat to 120ºC to avoid warpage
  - Solder refloows of component to be removed
  - Vacuum removal of component
  - Cleaning and preparation of PCB lands
  - Screening of fresh solder paste
  - Placement and reflow of new component
  - Inspection of solder joints

- The rework steps (except inspection) can be accomplished with high precision automated rework systems
Board Level Reliability (BLR)

- UTAC performed GQFN board level reliability following PCBA guidelines
  - GQFN package integrated daisy chain with PCB
- GQFN routable capability enables small package form factor with tight Die to package clearance
  - Reduction of package size up to 60% compared to QFN package
  - Increasing die to package ratio contributes higher CTE mismatch and risk thermal cycling on board reliability
Board Level Thermal Cycling Test

- Thermal Cycling Test is accelerated life test at extreme temperature range
  - To ascertain the solder attachment of surface mount assembly meet the reliability expectations in intended use environments
- Reference from IPC- 9701A
  - Air chamber, -40°C to 125°C with 15min dwell/ ramp, 1cyc/hr
Board Level Thermal Cycling Test

- GQFN 7x7mm, 162Balls units mounted on PCB to form integrated daisy chain for in-situ e-monitoring

<table>
<thead>
<tr>
<th>Package size (mm)</th>
<th>GQFN 7.0 x 7.0 x 0.75</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die size (mm)</td>
<td>4.2 x 4.2 x 0.203</td>
</tr>
<tr>
<td>Leadframe thickness (mm)</td>
<td>0.1</td>
</tr>
<tr>
<td>PCB (mm)</td>
<td>200x150x1.0 (4L- High Tg FR4)</td>
</tr>
<tr>
<td>Pre-solder</td>
<td>SAC305 (dia-0.25mm, standoff 0.1mm)</td>
</tr>
<tr>
<td>Daisy Chain</td>
<td>Lead to Lead bonding with Au wire</td>
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</tbody>
</table>
Board Level Thermal Cycling Test

- All units survived up to 1,100 temperature cycles without failures

Characteristic life 1,780 cycles

Failure mode
Board Level Drop Test

- To evaluate dropped performance of surface mount electronic components for handheld devices in an accelerated test environment
- Reference from JESD22-B111
  - 132x77x1.0mm 8-layers
  - Free-fall dropping
    - 1500 g’s deceleration,
    - Half-sine pulse duration of 0.5 millisecond
Board Level Drop Test

- All units pass 30 drops without failures

Characteristic life 420 cycles
PCB pad size impact on BLR

- PCB terminal pad size to be approximately a 1:1 ratio with the package lead
- Variation of the PCB pad size optional

(a) PCB pad is 25% larger than package terminal
(b) PCB pad is 65% larger than package terminal
PCB pad size impact on BLR

- Both pad options pass TMCL 1,000 cycles without failures
- The black data point in 2-parameter Weibull plot is case (a) and the characteristic life is 8% longer than case (b)
Conclusion

- GQFN’s routable leads and full grid array option provide a cost advantage per I/Os and better package performance (Thermal, Electrical, Reliability)

- GQFN packages following the SMT guidelines showed robust second level reliability

- GQFN is a qualified package and ramping up
Thank you!

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