FEATURES
HART-compliant fully integrated FSK modem
1200 Hz and 2200 Hz sinusoidal shift frequencies
115 μA maximum supply current in receive mode
Suitable for intrinsically safe applications
Integrated receive band-pass filter
   Minimal external components required
Clocking optimized for various system configurations
   Ultralow power crystal oscillator (60 μA maximum)
   External CMOS clock source
   Precision internal oscillator (AD5700-1 only)
Buffered HART output—extra drive capability
8 kV HBM ESD rating
1.71 V to 5.5 V power supply
1.71 V to 5.5 V interface
−40°C to +125°C operation
4 mm × 4 mm LFCSAP package
HART physical layer compliant
UART interface

APPLICATIONS
Field transmitters
HART multiplexers
PLC and DCS analog I/O modules
HART network connectivity

GENERAL DESCRIPTION
The AD5700/AD5700-1 are single-chip solutions, designed and specified to operate as a HART® FSK half-duplex modem, complying with the HART physical layer requirements. The AD5700/AD5700-1 integrate all of the necessary filtering, signal detection, modulating, demodulating and signal generation functions, thus requiring few external components. The 0.5% precision internal oscillator on the AD5700-1 greatly reduces the board space requirements, making it ideal for line-powered applications in both master and slave configurations. The maximum supply current consumption is 115 μA, making the AD5700/AD5700-1 an optimal choice for low power loop-powered applications. Transmit waveforms are phase continuous 1200 Hz and 2200 Hz sinusoids. The AD5700/AD5700-1 contain accurate carrier detect circuitry and use a standard UART interface.

Table 1. Related Products
<table>
<thead>
<tr>
<th>Part No.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD5755-1</td>
<td>Quad-channel, 16-bit, serial input, 4 mA to 20 mA and voltage output DAC, dynamic power control, HART connectivity</td>
</tr>
<tr>
<td>AD5421</td>
<td>16-bit, serial input, loop powered, 4 mA to 20 mA DAC</td>
</tr>
<tr>
<td>AD5410/</td>
<td>Single-channel, 12-bit/16-bit, serial input, 4 mA to 20 mA</td>
</tr>
<tr>
<td>AD5420</td>
<td>current source DACs</td>
</tr>
<tr>
<td>AD5412/1</td>
<td>Single-channel, 12-bit/16-bit, serial input, current source and voltage output DACs</td>
</tr>
</tbody>
</table>

![Functional Block Diagram](image-url)
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Added Figure 13 and Figure 14 ..................................... 10
Changes to External Crystal Section and Figure 25 .......... 15
5/13—Rev. C to Rev. D
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2/12—Revision 0: Initial Version

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### SPECIFICATIONS

$V_{CC} = 1.71$ V to 5.5 V, $IOV_{CC} = 1.71$ V to 5.5 V, AGND = DGND, CLKOUT disabled, HART_OUT with 5 nF load, internal and external receive filter, internal reference; all specifications are from $−40°C$ to $+125°C$ and relate to both A and B models, unless otherwise noted.

Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
</table>
| **POWER REQUIREMENTS**

  | $V_{CC}$ | 1.71 | 5.5 | V |
|-----------|--------|-----|-----|---|
  | $IOV_{CC}$ | 1.71 | 5.5 | V |
| $V_{CC}$ and $IOV_{CC}$ Current Consumption

  Demodulator

<table>
<thead>
<tr>
<th>86</th>
<th>115</th>
<th>µA</th>
<th>B model, external clock, $−40°C$ to $+85°C$</th>
</tr>
</thead>
<tbody>
<tr>
<td>179</td>
<td>µA</td>
<td>B model, external clock, $−40°C$ to $+125°C$</td>
<td></td>
</tr>
<tr>
<td>69</td>
<td>97</td>
<td>µA</td>
<td>B model, external clock, $−40°C$ to $+85°C$, external reference</td>
</tr>
<tr>
<td>157</td>
<td>µA</td>
<td>B model, external clock, $−40°C$ to $+125°C$, external reference</td>
<td></td>
</tr>
</tbody>
</table>
| Modulator

<table>
<thead>
<tr>
<th>124</th>
<th>140</th>
<th>µA</th>
<th>B model, external clock, $−40°C$ to $+85°C$</th>
</tr>
</thead>
<tbody>
<tr>
<td>193</td>
<td>µA</td>
<td>B model, external clock, $−40°C$ to $+125°C$</td>
<td></td>
</tr>
<tr>
<td>73</td>
<td>96</td>
<td>µA</td>
<td>B model, external clock, $−40°C$ to $+85°C$, external reference</td>
</tr>
<tr>
<td>153</td>
<td>µA</td>
<td>B model, external clock, $−40°C$ to $+125°C$, external reference</td>
<td></td>
</tr>
<tr>
<td>270</td>
<td>µA</td>
<td>A model, external clock, $−40°C$ to $+125°C$</td>
<td></td>
</tr>
</tbody>
</table>

#### Crystal Oscillator

<table>
<thead>
<tr>
<th>33</th>
<th>60</th>
<th>µA</th>
<th>External crystal, 16 pF at XTAL1 and XTAL2</th>
</tr>
</thead>
<tbody>
<tr>
<td>44</td>
<td>71</td>
<td>µA</td>
<td>External crystal, 36 pF at XTAL1 and XTAL2</td>
</tr>
</tbody>
</table>

#### Internal Oscillator

<table>
<thead>
<tr>
<th>218</th>
<th>285</th>
<th>µA</th>
</tr>
</thead>
</table>
| Power-Down Mode

  | 16 | 35 | µA | Internal reference disabled, $−40°C$ to $+85°C$ |
|-----|-----|----|
  | 75 | µA | Internal reference disabled, $−40°C$ to $+125°C$ |

#### INTERNAL VOLTAGE REFERENCE

<table>
<thead>
<tr>
<th>Internal Reference Voltage</th>
<th>1.47</th>
<th>1.5</th>
<th>1.52</th>
<th>V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load Regulation</td>
<td>18</td>
<td>ppm/µA</td>
<td>Tested with 50 µA load</td>
<td></td>
</tr>
</tbody>
</table>

#### OPTIONAL EXTERNAL VOLTAGE REFERENCE

<table>
<thead>
<tr>
<th>External Reference Input Voltage</th>
<th>2.47</th>
<th>2.5</th>
<th>2.53</th>
<th>V</th>
</tr>
</thead>
</table>
| External Reference Input Current

  Demodulator

<table>
<thead>
<tr>
<th>16</th>
<th>21</th>
<th>µA</th>
</tr>
</thead>
<tbody>
<tr>
<td>28</td>
<td>33</td>
<td>µA</td>
</tr>
<tr>
<td>5.5</td>
<td>7</td>
<td>µA</td>
</tr>
<tr>
<td>Power-Down</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

  | 4.6 | 8.6 | µA |

#### DIGITAL INPUTS

<table>
<thead>
<tr>
<th>$V_{IH}$, Input High Voltage</th>
<th>$0.7 \times IOV_{CC}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IL}$, Input Low Voltage</td>
<td>$0.3 \times IOV_{CC}$</td>
</tr>
<tr>
<td>Input Current</td>
<td>−0.1</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>5</td>
</tr>
<tr>
<td>Parameter1</td>
<td>Min</td>
</tr>
<tr>
<td>------------</td>
<td>-----</td>
</tr>
<tr>
<td><strong>DIGITAL OUTPUTS</strong></td>
<td></td>
</tr>
<tr>
<td>VOH, Output High Voltage</td>
<td>IOVCC − 0.5</td>
</tr>
<tr>
<td>VOL, Output Low Voltage</td>
<td>0.4</td>
</tr>
<tr>
<td>CD Assert6</td>
<td>85</td>
</tr>
<tr>
<td><strong>HART_IN INPUT</strong></td>
<td></td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1.5</td>
</tr>
<tr>
<td><strong>HART_OUT OUTPUT</strong></td>
<td></td>
</tr>
<tr>
<td>Output Voltage</td>
<td>459</td>
</tr>
<tr>
<td>Mark Frequency7</td>
<td>1200</td>
</tr>
<tr>
<td>Space Frequency7</td>
<td>2200</td>
</tr>
<tr>
<td>Frequency Error</td>
<td>−0.5</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Phase Continuity Error6</td>
<td>0</td>
</tr>
<tr>
<td>Maximum Load Current5</td>
<td>160</td>
</tr>
<tr>
<td>Transmit Impedance</td>
<td>7</td>
</tr>
<tr>
<td>70</td>
<td></td>
</tr>
<tr>
<td><strong>INTERNAL OSCILLATOR</strong></td>
<td></td>
</tr>
<tr>
<td>Frequency</td>
<td>1.2226</td>
</tr>
<tr>
<td>1.2165</td>
<td>1.2288</td>
</tr>
<tr>
<td><strong>EXTERNAL CLOCK</strong></td>
<td></td>
</tr>
<tr>
<td>External Clock Source Frequency</td>
<td>3.6496</td>
</tr>
</tbody>
</table>

1. Temperature range: −40°C to +125°C, typical at 25°C.
2. Current consumption specifications are based on mean current values.
3. The demodulator and modulator currents are specified using an external clock. If using an external crystal oscillator, the crystal oscillator current specification must be added to the corresponding VCC and IOVCC demodulator/modulator current specification to obtain the total supply current required in this mode.
4. The demodulator and modulator currents are specified using an external clock. If using the internal oscillator, the internal oscillator current specification must be added to the corresponding VCC and IOVCC demodulator/modulator current specification to obtain the total supply current required in this mode.
5. Guaranteed by design and characterization, but not production tested.
6. Specification set assuming a sinusoidal input signal containing preamble characters at the input and an ideal external filter (see Figure 23).
7. If the internal oscillator is not used, frequency accuracy is dependent on the accuracy of the crystal or clock source used.
TIMING CHARACTERISTICS

$V_{CC} = 1.71\, V$ to 5.5\, V, $IOV_{CC} = 1.71\, V$ to 5.5\, V, $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter 1</th>
<th>Limit at $T_{MIN}$, $T_{MAX}$</th>
<th>Unit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_1$</td>
<td>1</td>
<td>Bit time$^2$ max</td>
<td>Carrier start time. Time from RTS falling edge to carrier reaching its first peak. See Figure 3.</td>
</tr>
<tr>
<td>$t_2$</td>
<td>1</td>
<td>Bit time$^2$ max</td>
<td>Carrier stop time. Time from RTS rising edge to carrier amplitude dropping below the minimum receive amplitude.</td>
</tr>
<tr>
<td>$t_3$</td>
<td>1</td>
<td>Bit time$^2$ max</td>
<td>Carrier decay time. Time from RTS rising edge to carrier amplitude dropping to ac zero. See Figure 4.</td>
</tr>
<tr>
<td>$t_4$</td>
<td>6</td>
<td>Bit times$^2$ max</td>
<td>Carrier detect on. Time from carrier on to CD rising edge. See Figure 5.</td>
</tr>
<tr>
<td>$t_5$</td>
<td>6</td>
<td>Bit times$^2$ max</td>
<td>Carrier detect off. Time from carrier off to CD falling edge. See Figure 6.</td>
</tr>
<tr>
<td>$t_6$</td>
<td>10</td>
<td>Bit times$^2$ max</td>
<td>Carrier detect on when switching from transmit mode to receive mode in the presence of a constant valid carrier. Time from RTS rising edge to CD rising edge. See Figure 7.</td>
</tr>
<tr>
<td>$t_7$</td>
<td>2.1 ms typ</td>
<td></td>
<td>Crystal oscillator power-up time. On application of a valid power supply voltage at $V_{CC}$ or on enabling of the oscillator via the XTAL_EN pin. Crystal load capacitors = 16 pF.</td>
</tr>
<tr>
<td>$t_8$</td>
<td>6 ms typ</td>
<td></td>
<td>Crystal oscillator power-up time. Crystal load capacitors = 36 pF.</td>
</tr>
<tr>
<td>$t_9$</td>
<td>25 µs typ</td>
<td></td>
<td>Internal oscillator power-up time. On application of a valid power supply voltage at $V_{CC}$ or on enabling of the oscillator via the CLK_CFG0 and CLK_CFG1 pins.</td>
</tr>
<tr>
<td>$t_{10}$</td>
<td>10 ms typ</td>
<td></td>
<td>Reference power-up time.</td>
</tr>
<tr>
<td>$t_{11}$</td>
<td>30 µs typ</td>
<td></td>
<td>Transition time from power-down mode to normal operating mode (external clock source, external reference).</td>
</tr>
</tbody>
</table>

$^1$ Specifications apply to AD5700/AD5700-1 configured with internal or external receive filter.

$^2$ Bit time is the length of time to transfer one bit of data (1 bit time = $1/1200\, Hz = 833.333\, \mu s$).
ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ C$, unless otherwise noted.
Transient currents of up to 100 mA do not cause SCR latch-up.

Table 4.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$ to GND</td>
<td>$-0.3 \text{ V} \text{ to } +7 \text{ V}$</td>
</tr>
<tr>
<td>$IOV_{CC}$ to GND</td>
<td>$-0.3 \text{ V} \text{ to } +7 \text{ V}$</td>
</tr>
<tr>
<td>Digital Inputs to DGND</td>
<td>$-0.3 \text{ V} \text{ to } IOV_{CC} + 0.3 \text{ V} \text{ or } +7 \text{ V (whichever is less)}$</td>
</tr>
<tr>
<td>Digital Output to DGND</td>
<td>$-0.3 \text{ V} \text{ to } IOV_{CC} + 0.3 \text{ V} \text{ or } +7 \text{ V (whichever is less)}$</td>
</tr>
<tr>
<td>HART_OUT to AGND</td>
<td>$-0.3 \text{ V} \text{ to } +2.5 \text{ V}$</td>
</tr>
<tr>
<td>HART_IN to AGND</td>
<td>$-0.3 \text{ V} \text{ to } V_{CC} + 0.3 \text{ V} \text{ or } +7 \text{ V (whichever is less)}$</td>
</tr>
<tr>
<td>ADC_IP</td>
<td>$-0.3 \text{ V} \text{ to } V_{CC} + 0.3 \text{ V} \text{ or } +7 \text{ V (whichever is less)}$</td>
</tr>
<tr>
<td>AGND to DGND</td>
<td>$-0.3 \text{ V} \text{ to } +0.3 \text{ V}$</td>
</tr>
</tbody>
</table>

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

<table>
<thead>
<tr>
<th>Package Type</th>
<th>$\theta_{JA}$</th>
<th>$\theta_{JC}$</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>24-Lead LF CSP</td>
<td>56</td>
<td>3</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

1 Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
## Table 6. Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>XTAL_EN</td>
<td>Crystal Oscillator Circuit Enable. A low state enables the crystal oscillator circuit, and an external crystal is required. A high state disables the crystal oscillator circuit, and an external clock source or the internal oscillator (AD5700-1 only) provides the clock source. This pin is used in conjunction with the CLK_CFG0 and CLK_CFG1 pins in configuring the required clock generation scheme.</td>
</tr>
<tr>
<td>2</td>
<td>CLKOUT</td>
<td>Clock Output. If using the crystal oscillator or the internal RC oscillator, a clock output can be configured at the CLKOUT pin. Enabling the clock output consumes extra current to drive the load on this pin. See the CLKOUT section for more details.</td>
</tr>
<tr>
<td>3</td>
<td>CLK_CFG0</td>
<td>Clock Configuration Control. See Table 7.</td>
</tr>
<tr>
<td>4</td>
<td>CLK_CFG1</td>
<td>Clock Configuration Control. See Table 7.</td>
</tr>
<tr>
<td>5</td>
<td>RESET</td>
<td>Active Low Digital Input. Holding RESET low places the AD5700/AD5700-1 in power-down mode. A high state on RESET returns the AD5700/AD5700-1 to their power-on state. If not using this pin, tie this pin to IOVCC.</td>
</tr>
<tr>
<td>6</td>
<td>CD</td>
<td>Carrier Detect—Digital Output. A high on CD indicates a valid carrier is detected.</td>
</tr>
<tr>
<td>7</td>
<td>TXD</td>
<td>Transmit Data—Digital Input. Data input to the modulator.</td>
</tr>
<tr>
<td>8</td>
<td>RTS</td>
<td>Request to Send—Digital Input. A high state enables the demodulator and disables the modulator. A low state enables the modulator and disables the demodulator.</td>
</tr>
<tr>
<td>9</td>
<td>DUPLEX</td>
<td>A high state on this pin enables full duplex operation. See the Theory of Operation section. A low state disables this feature.</td>
</tr>
<tr>
<td>10</td>
<td>RXD</td>
<td>Receive Data—UART Interface Digital Data Output. Data output from the demodulator is accessed on this pin.</td>
</tr>
<tr>
<td>11</td>
<td>IOVcc</td>
<td>Digital Interface Supply. Digital threshold levels are referenced to the voltage applied to this pin. The applied voltage can be in the range of 1.71 V to 5.5 V. IOVcc should be decoupled to ground with low ESR 10 μF and 0.1 μF capacitors (see the Supply Decoupling section).</td>
</tr>
<tr>
<td>12</td>
<td>DGND</td>
<td>Digital Circuity Ground Reference Connection. For typical operation, it is recommended to connect this pin to AGND.</td>
</tr>
<tr>
<td>13</td>
<td>REG_CAP</td>
<td>Capacitor Connection for Internal Voltage Regulator. Connect a 1 μF capacitor from this pin to ground.</td>
</tr>
<tr>
<td>14</td>
<td>HART_OUT</td>
<td>HART FSK Signal Output. See the FSK Modulator section and Figure 30 for typical connections.</td>
</tr>
<tr>
<td>15</td>
<td>REF</td>
<td>Internal Reference Voltage Output, or External 2.5 V Reference Voltage Input. Connect a 1 μF capacitor from this pin to ground. When supplying an external reference, the Vcc supply requires a minimum voltage of 2.7 V.</td>
</tr>
<tr>
<td>16</td>
<td>HART_IN</td>
<td>HART FSK Signal. When using the internal filter, couple the HART input signal into this pin using a 2.2 nF series capacitor. If using an external band-pass filter as shown in Figure 23, do not connect to this pin.</td>
</tr>
<tr>
<td>17</td>
<td>ADC_IP</td>
<td>If using the internal band-pass filter, connect 680 pF to this pin. Alternatively, this pin allows direct connection to the ADC input, in which case an external band-pass filter network must be used, as shown in Figure 23.</td>
</tr>
<tr>
<td>18</td>
<td>Vcc</td>
<td>Power Supply Input. 1.71 V to 5.5 V can be applied to this pin. Vcc should be decoupled to ground with low ESR 10 μF and 0.1 μF capacitors (see the Supply Decoupling section).</td>
</tr>
<tr>
<td>Pin No.</td>
<td>Mnemonic</td>
<td>Description</td>
</tr>
<tr>
<td>---------</td>
<td>----------</td>
<td>-------------</td>
</tr>
<tr>
<td>19</td>
<td>AGND</td>
<td>Analog Circuitry Ground Reference Connection.</td>
</tr>
<tr>
<td>20</td>
<td>XTAL2</td>
<td>Connection for External 3.6864 MHz Crystal. Do not connect to this pin if using the internal RC oscillator (AD5700-1 only) or an external clock source.</td>
</tr>
<tr>
<td>21</td>
<td>XTAL1</td>
<td>Connection for External 3.6864 MHz Crystal or External Clock Source Input. Tie this pin to ground if using the internal RC oscillator (AD5700-1 only).</td>
</tr>
<tr>
<td>22</td>
<td>DGND</td>
<td>Digital Circuitry Ground Reference Connection. For typical operation, it is recommended to connect this pin to AGND.</td>
</tr>
<tr>
<td>23</td>
<td>REF_EN</td>
<td>Reference Enable. A high state enables the internal 1.5 V reference and buffer. A low state disables the internal reference and input buffer, and a buffered external 2.5 V reference source must be applied at REF. If REF_EN is tied low, $V_{CC}$ must be greater than 2.7 V.</td>
</tr>
<tr>
<td>24</td>
<td>FILTER_SEL</td>
<td>Band-Pass Filter Select. A high state enables the internal filter and the HART signal should be applied to the HART_IN pin. A low state disables the internal filter and an external band-pass filter must then be connected at the ADC_IP input pin. In this case, the HART signal should be applied to the ADC_IP pin.</td>
</tr>
<tr>
<td>EPAD</td>
<td>EPAD</td>
<td>Exposed Pad. For typical operation, it is recommended to connect this pin to AGND.</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS

Figure 3. Carrier Start Time

Figure 4. Carrier Stop/Decay Time

Figure 5. Carrier Detect On Timing

Figure 6. Carrier Detect Off Timing

Figure 7. Carrier Detect on When Switching from Transmit Mode to Receive Mode in the Presence of a Constant Valid Carrier

Figure 8. Supply Currents vs. Supply Voltage—External Reference
Figure 9. Supply Currents vs. Supply Voltage—Internal Reference

Figure 10. Current in Tx Mode vs. Resistive Load

Figure 11. Current in Tx Mode vs. Capacitive Load

Figure 12. Input Filter Frequency Response

Figure 13. Carrier Detect—Voltage vs. Current, 2 V

Figure 14. Carrier Detect—Voltage vs. Current, 3.3 V
Figure 15. Reference Voltage vs. VCC

Figure 16. Reference Voltage vs. Temperature

Figure 17. HART_OUT Voltage vs. RLOAD

Figure 18. HART_OUT Voltage vs. CLOAD
TERMINOLOGY

VCC and IOVCC Current Consumption
This specification gives a summation of the current consumption of both the VCC and the IOVCC supplies. Figure 11 shows separate measurements for VCC and IOVCC currents vs. varying capacitive loads, in transmit mode.

Load Regulation
Load regulation is the change in reference output voltage due to a specified change in load current. It is expressed in ppm/µA.

CD Assert
The minimum value at which the carrier detect signal asserts is 85 mV p-p and the maximum value it asserts at is 110 mV p-p. CD is already high (asserted) for HART input signals greater than 110 mV p-p. This specification was set assuming a sinusoidal input signal containing preamble characters at the input and an ideal external filter (see Figure 23).

HART_OUT Output Voltage
This is the peak-to-peak HART_OUT output voltage. The specification in Table 2 was set using a worst-case load of 160 Ω, ac-coupled with a 2.2 µF capacitor. Figure 17 and Figure 18 show HART_OUT output voltages for both resistive and purely capacitive loads.

Mark/Space Frequency
A 1.2 kHz signal represents a digital 1, or mark, whereas a 2.2 kHz signal represents a 0, or space.

Phase Continuity Error
The DDS engine in this design inherently generates continuous phase signals, thus avoiding any output discontinuity when switching between frequencies. This attribute is desirable for signals that are to be transmitted over a band limited channel, because discontinuities in a signal introduce wideband frequency components. As the name suggests, for a signal to be continuous, the phase continuity error must be 0°.
THEORY OF OPERATION

Highway Addressable Remote Transducer (HART) Communication is the global standard for sending and receiving digital information across analog wires between smart field devices and control systems. This is a digital two-way communication system, in which a 1 mA p-p frequency shift keyed (FSK) signal is modulated on top of a 4 mA to 20 mA analog current signal. The AD5700/AD5700-1 are designed and specified to operate as a single-chip, low power, HART FSK half-duplex modem, complying with the HART physical layer requirements (Revision 8.1).

A single-chip solution, the AD5700/AD5700-1 not only integrate the modulation and demodulation functions, but also contain an internal reference, an integrated receive band-pass filter (which has the flexibility of being bypassed if required), and an internally buffered HART output, giving a high output drive capability and removing the need for external buffering. The AD5700-1 option also contains a precision internal RC oscillator. The block diagram in Figure 1 shows a graphical illustration of how these circuit blocks are connected together. As a result of such extensive integration options, minimal external components are required. The AD5700/AD5700-1 are suitable for use in both HART field instrument and master configurations.

The AD5700/AD5700-1 either transmit or receive 1.2 kHz and 2.2 kHz carrier signals. A 1.2 kHz signal represents a digital 1, or mark, whereas a 2.2 kHz signal represents a 0, or space. There are three main clocking configurations supported by these parts, two of which are available on the AD5700 option, whereas all three are available on the AD5700-1 device:

- External crystal
- CMOS clock input
- Internal RC oscillator (AD5700-1 only)

The device is controlled via a standard UART interface. The relevant signals are RTS, CD, TXD, and RXD (see Table 6 for more detail on individual pin descriptions).

FSK MODULATOR

The modulator converts a bit stream of UART-encoded HART data at the TXD input to a sequence of 1200 Hz and 2200 Hz tones (see Figure 19). This sinusoidal signal is internally buffered and output on the HART_OUT pin. The modulator is enabled by bringing the RTS signal low.

The modulator block contains a DDS engine that produces a 1.2 kHz or 2.2 kHz sine wave in digital form and then performs a digital-to-analog conversion. This DDS engine inherently generates continuous phase signals, thus avoiding any output discontinuity when switching between frequencies. For more information on DDS fundamentals, see MT-085, Fundamentals of Direct Digital Synthesizers (DDS). Figure 20 demonstrates a simple implementation of this FSK encoding.
CONNECTING TO HART_OUT

The HART_OUT pin is dc biased to 0.75 V and should be capacitively coupled to the load. The current consumption specifications in Table 2 are based on driving a 5 nF load. If the application requires a larger load value, more current is required. This value can be calculated from the following formula:

\[
I_{TOTAL} = I_{AD5700} + I_{LOAD RMS}
\]

\[
I_{LOAD RMS} = \frac{500 \text{ mV}}{4 \sqrt{2} \times \left( \frac{1}{2\pi f C_{LOAD}} \right)^2 + R_{LOAD}^2}
\]

(1)

where:

\(I_{AD5700}\) is the current drawn by the AD5700/AD5700-1 in transmit mode as per specifications (see Table 2). Note that the specifications in Table 2 assume a 5 nF \(C_{LOAD}\).

\(f\) is the output frequency (1.2 kHz or 2.2 kHz).

\(C_{LOAD}\) is the capacitive load to ground on HART_OUT.

\(R_{LOAD}\) is the resistive load on the loop.

When driving a purely capacitive load, the load should be in the range of 5 nF to 52 nF. See Figure 11 for a typical plot of supply current vs. capacitive load.

**Example**

Assume use of an internal reference, and \(C_{LOAD} = 52 \text{ nF}\):

\(I_{CC} + IO_{CC} = 140 \mu\text{A} \text{ maximum (from Table 2 specification)}\)

Note that this is incorporating a 5 nF load.

Therefore, to calculate the load current required to drive the extra 47 nF, use Equation 1.

Substituting \(f = 1200 \text{ Hz}, C_{LOAD} = 47 \text{ nF}, \) and \(R_{LOAD} = 0 \Omega\) into the formula results in \(I_{LOAD}\) of 31.3 \(\mu\text{A}\).

If using the crystal oscillator, this adds 60 \(\mu\text{A}\) maximum (see Table 2 for conditions).

Thus, the total worst-case current in this example is:

140 \(\mu\text{A}\) + 31.3 \(\mu\text{A}\) + 60 \(\mu\text{A}\) = 231.3 \(\mu\text{A}\)

If driving a load with a resistive element, it is recommended to place a 22 nF capacitor to ground at the HART_OUT pin. The load should be coupled with a 2.2 \(\mu\text{F}\) series capacitor. For low impedance devices, the \(R_{LOAD}\) range is typically 230 \(\Omega\) to 600 \(\Omega\).

---

FSK DEMODULATOR

When RTS is logic high, the modulator is disabled and the demodulator is enabled, that is, the AD5700/AD5700-1 are in receive mode. A high on CD indicates a valid carrier is detected. The demodulator accepts an FSK signal at the HART_IN pin and restores the original modulated signal at the UART interface digital data output pin, RXD. The combination of the ADC, digital filtering and digital demodulation results in a highly accurate output on the RXD pin. The HART bit stream follows a standard UART frame with a start bit, 8-bit data, one parity, and a stop bit (see Figure 22).

CONNECTING TO HART_IN OR ADC_IP

The AD5700/AD5700-1 have two filter configuration options: an external filter (HART signal is applied to ACP_IP) and an internal filter (HART signal is applied to HART_IN).

The external filter configuration is shown in Figure 23. In this case, the HART signal is applied to the ADC_IP pin through an external filter circuit. In safety critical applications, the AD5700/AD5700-1 must be isolated from the high voltage of the loop supply. The recommended external band-pass filter includes a 150 k\(\Omega\) resistor, which limits current to a sufficiently low level to adhere to intrinsic safety requirements. In this case, the input has higher transient voltage protection and should, therefore, not require additional protection circuitry, even in the most demanding of industrial environments. Assuming the use of a 1% accurate resistor and 10% accurate capacitor components, the calculated variation in CD trip voltage levels vs. the ideal is ±3.5 mV.
The internal filter configuration is shown in Figure 24. This option is beneficial where cost or board space is a large concern because it removes the need for multiple external components. This configuration achieves an 8 kV ESD HBM rating but requires extra external protection circuitry for EMC and surge protection purposes if used in harsh industrial environments.

**CLOCK CONFIGURATION**

The AD5700/AD5700-1 support numerous clocking configurations to allow the optimal trade-off between cost and power:

- External crystal
- CMOS clock input
- Internal RC oscillator (AD5700-1 only)

The CLK_CFG0, CLK_CFG1, and XTAL_EN pins configure the clock generation as shown in Table 7. The AD5700/AD5700-1 can also provide a clock output at CLKOUT (for more details, see the CLKOUT section).

**External Crystal**

The typical connection for an external crystal (ABLS-3.6864MHZ-L4Q-T) is shown in Figure 25. To ensure minimum current consumption and to minimize stray capacitances, connections between the crystal, capacitors, and ground should be made as close to the AD5700/AD5700-1 as possible. Consult individual crystal vendors for recommended load information and crystal performance specifications.

![Figure 25. Crystal Oscillator Connection](image)

The ABLS-3.6864MHZ-L4Q-T crystal oscillator data sheet recommended two 36 pF capacitors. Because the crystal current consumption is dominated by the load capacitance, in an effort to reduce the crystal current consumption, two 16 pF capacitors were used on the XTAL1 and XTAL2 pins. The AD5700/AD5700-1 still functioned as expected, even with the resulting reduction in frequency performance from the crystal due to the smaller capacitance values. Crystals are available that support 16 pF capacitors. It is recommended to consult the relevant crystal manufacturers for this information.

**CMOS Clock Input**

A CMOS clock input can also be used to generate a clock for the AD5700/AD5700-1. To use this mode, connect an external clock source to the XTAL 1 pin, and leave XTAL2 open circuit (see Figure 26).

![Figure 26. CMOS Clock Connection](image)

**Internal Oscillator (AD5700-1 only)**

Consuming typically 218 µA, the low power, internal, 0.5 % precision RC oscillator, available only on the AD5700-1, has an oscillation frequency of 1.2288 MHz. To use this mode, tie the XTAL1 pin to ground and leave the XTAL2 pin open circuit (see Figure 27).

![Figure 27. Internal Oscillator Connection](image)

**CLKOUT**

The AD5700/AD5700-1 can provide a clock output at CLKOUT (see Table 7).

- If using the crystal oscillator, this clock output can be configured as a 3.6864 MHz, 1.8432 MHz, or 1.2288 MHz buffer clock.
- If using a CMOS clock, no clock output can be configured at the CLKOUT pin.
- If using the internal RC oscillator, this clock output is only available as a 1.2288 MHz buffer clock.

The amplitude of the clock output depends on the IOVCC level; therefore, the clock output can be in the range of 1.71 V p-p to 5.5 V p-p. Enabling the clock output of the AD5700/AD5700-1 increases the current consumption of the device. This increase is due to the current required to drive any load at the CLKOUT pin, which should not be more than 30 pF.

This capacitance should be minimized to reduce current consumption and provide the clock with the cleanest edges. The additional current drawn from the IOVCC supply can be calculated using the following equation:

\[ I = C \times V \times f \]
Table 7. Clock Configuration Options

<table>
<thead>
<tr>
<th>XTAL_EN</th>
<th>CLK_CFG1</th>
<th>CLK_CFG0</th>
<th>CLKOUT</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>No output</td>
<td>3.6864 MHz CMOS clock connected at XTAL1 pin</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>No output</td>
<td>1.2288 MHz CMOS clock connected at XTAL1 pin</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>No output</td>
<td>Internal oscillator enabled (AD5700-1 only)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1.2288 MHz output</td>
<td>Internal oscillator enabled, CLKOUT enabled (AD5700-1 only)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>No output</td>
<td>Crystal oscillator enabled</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>3.6864 MHz output</td>
<td>Crystal oscillator enabled, CLKOUT enabled</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1.8432 MHz output</td>
<td>Crystal oscillator enabled, CLKOUT enabled</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1.2288 MHz output</td>
<td>Crystal oscillator enabled, CLKOUT enabled</td>
</tr>
</tbody>
</table>

SUPPLY CURRENT CALCULATIONS

The $V_{CC}$ and $IOV_{CC}$ current consumption specifications shown in Table 2 are derived using the internal reference and an external clock source. This specification is given for a maximum temperature of 85°C (115 µA receive current and 140 µA transmit current) and an extended maximum temperature of 125°C (179 µA receive current and 193 µA transmit current). Alternatively, if the external reference is preferred, (assuming a maximum temperature of 85°C), the receive and transmit supply current values become 118 µA and 129 µA respectively, including the current required by the external reference. A similar calculation can be done for the 125°C maximum temperature case.

If the crystal oscillator or internal oscillator is used, $V_{CC}$ and $IOV_{CC}$ current consumption figures return to the 115 µA receive current and 140 µA transmit current. However, the resultant current consumption from the crystal oscillator or internal oscillator must now be accounted for, 60 µA maximum additional current for the crystal oscillator, or 285 µA maximum additional current for the internal oscillator option. This gives a maximum current consumption of 175 µA in receive mode and 200 µA in transmit mode, when using the internal reference and the crystal oscillator. Utilizing the internal reference and the internal oscillator (AD5700-1 only) results in a total maximum current consumption of 400 µA for receive current and 425 µA for transmit current.

POWER-DOWN MODE

The AD5700/AD5700-1 can be placed into power-down mode by holding the $\text{RESET}$ pin low. If using the internal reference, it is recommended to tie the $\text{REF}_\text{EN}$ pin to the $\text{RESET}$ pin so that it is also powered down. If the reference is not powered down while $\text{RESET}$ is low, the output voltage on the $\text{REF}$ pin is approximately 1.7 V until $\text{RESET}$ is brought high again.

In this mode, the receive, transmit, and oscillator circuits are all switched off, and the device consumes a typical current of 16 µA.

FULL DUPLEX OPERATION

Full duplex operation means that the modulator and demodulator of the AD5700/AD5700-1 are enabled at the same time. This is a powerful feature, enabling a self-test procedure of not only the HART device but also the complete signal path between the HART device and the host controller. This provides verification that the local communications loop is functional. This increased level of system diagnostics is useful in production self-test and is advantageous in improving the application's safety integrity level (SIL) rating. The full duplex mode of operation is enabled by connecting the $\text{DUPLEX}$ pin to logic high.
APPLICATIONS INFORMATION

SUPPLY DECOUPLING

It is recommended to decouple the VCC and IOVCC supplies with 10 μF in parallel with 0.1 μF capacitors to ground. For many applications, 1 μF in parallel with 0.1 μF ceramic capacitors to ground should be sufficient. The REG_CAP voltage of 1.8 V is used to supply the AD5700/AD5700-1 internal circuitry and is derived from the VCC supply using a high efficiency clocking LDO. Decouple this REG_CAP supply with a 1 μF ceramic capacitor to ground. It is also required to decouple the REF pin with a 1 μF ceramic capacitor to ground. Place decoupling capacitors as close to the relevant pins as possible.

For loop-powered applications, it is recommended to connect a resistance in series with the VCC supply to minimize the effect of any noise, which may, depending on the system configuration, be introduced onto the loop as a result of current draw variations from the AD5700/AD5700-1. For typical applications, 470 Ω of resistance has proven most effective. However, depending on the application conditions, alternative values may also be acceptable (see R1 in Figure 31).

TRANSIENT VOLTAGE PROTECTION

Many industrial control applications have requirements for HART-enabled current input and output modules. Figure 28 shows an example of a HART-enabled current input module that contains transient voltage protection circuitry, which is very important in harsh industrial control environments.

The module is powered from a 24 V field supply, and the 250 Ω load is within the low impedance module itself. This configuration is in contrast to Figure 29, which demonstrates a secondary HART device, in which the load is outside of the module. For transient voltage protection, a 10 V unidirectional (for protection against positive high voltage transients) transient voltage suppressor (TVS) is placed at the connection point of the current input module. The TVS component that is used in a given application circuit must have power ratings that are appropriate to the individual system. When choosing the TVS, low leakage current is also an important specification for maintaining the accuracy of the analog current input. In the event of a transient spike, the 22 Ω series resistor acts as a current limiting resistor for the FSK output pin. The FSK input pin is inherently protected by the 150 kΩ resistor, which forms part of the recommended external filter circuitry at the FSK input. The voltage divider, made up of both a 75 kΩ resistor and a 22 kΩ resistor, is used to maintain a 0.75 V dc bias at the field side of the FSK output switch.

Figure 28. Current Input Module, HART Circuit

Figure 29. Secondary HART Device
As previously mentioned, Figure 29 shows an example secondary HART device, incorporating two-stage protection circuitry. In this example, a bidirectional (for protection against both positive and negative high voltage transients) TVS is included to provide flexibility in the polarity of the connection points of the module. Because this module could be connected to any point on the current loop, the higher TVS rating was chosen. The lower rated second stage provides added protection for the AD5700/AD5700-1 device.

**TYPICAL CONNECTION DIAGRAMS**

Figure 30 shows a typical connection diagram for the AD5700/AD5700-1 using the external and internal options. See the Connecting to HART_IN or ADC_IP section for more details.

The AD5700/AD5700-1 are designed to interface easily with Analog Devices, Inc., innovative portfolio of industrial converters like the AD5421 loop-powered current-output DAC, the AD5410/AD5420 and AD5412/AD5422 family of line-powered current-output DACs, and the AD5755-1, a quad DAC with innovative dynamic power control technology. The combination of Analog Devices industrial converters and the AD5700/AD5700-1 greatly simplifies system design, enhancing reliability while reducing overall PCB size.

Figure 31 shows how the AD5700/AD5700-1 HART modem can be interfaced with the AD5421 (4 mA to 20 mA loop-powered DAC) and the ADuCM360 microcontroller to construct a loop powered transmitter circuit. The HART signal from HART_OUT is introduced to the AD5421 via the CIN pin.

The HART enabled smart transmitter reference demo circuit (the block diagram shown in Figure 32) was developed by Analog Devices and uses the AD5421, a 16-bit, loop-powered, 4 mA to 20 mA DAC, the ADuCM360 microcontroller and the AD5700 modem. This circuit has been compliance tested, verified, and registered as an approved HART solution by the HART Communication Foundation. Contact your sales representative for further information about this demo circuit.

In conclusion, the AD5700/AD5700-1 enable quick and easy deployment of a robust HART-compliant system.
Figure 31. Loop-Powered Transmitter Diagram
Figure 32. Block Diagram—Analog Devices HART-Enabled Smart Transmitter Reference Demo Circuit
### OUTLINE DIMENSIONS

**Figure 33. 24-Lead Lead Frame Chip Scale Package (LFCSP_WQ)**

4 mm × 4 mm Body, Very Thin Quad (CP-24-10)

Dimensions shown in millimeters

### ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Oscillator Options</th>
<th>Receive Supply Current</th>
<th>Package Description</th>
<th>Package Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD5700BCPZ-R5</td>
<td>−40°C to +125°C</td>
<td>External clock, crystal</td>
<td>157 μA</td>
<td>24-Lead LFCSP_WQ</td>
<td>CP-24-10</td>
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<tr>
<td>AD5700BCPZ-RL7</td>
<td>−40°C to +125°C</td>
<td>External clock, crystal</td>
<td>157 μA</td>
<td>24-Lead LFCSP_WQ</td>
<td>CP-24-10</td>
</tr>
<tr>
<td>AD5700ACPZ-RL7</td>
<td>−40°C to +125°C</td>
<td>External clock, crystal or internal oscillator</td>
<td>260 μA</td>
<td>24-Lead LFCSP_WQ</td>
<td>CP-24-10</td>
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<tr>
<td>AD5700-1BCPZ-R5</td>
<td>−40°C to +125°C</td>
<td>External clock, crystal or internal oscillator</td>
<td>442 μA</td>
<td>24-Lead LFCSP_WQ</td>
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<td>Evaluation Board for AD5700 and AD5700-1</td>
<td>CP-24-10</td>
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</table>

1 Z = RoHS Compliant Part.