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A Highly Reliable Flip Chip Solution based on Electroplated AuSn Bumps in a Leadless Package

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Abstract

We introduce an innovative flip chip in package concept based on small electroplated AuSn bumps as first level interconnect. Reliability studies prove the compliance of the leadless package concept to high quality standards, which include moisture sensitivity level 1 (MSL1), temperature cycling on board, shock tests as well as autoclave tests. Detailed SEM and TEM investigations demonstrate an excellent quality of the different interfaces. The package concept meets current packaging requirements, such as small form factor, environmental friendliness (green package), RF capability and low cost production. The flip chip in package concept, demonstrated here for small pin counts, has further potential to be extended to a medium pin count range.

1. Introduction

Trends for package developments can be found in various international roadmaps, for example ITRS, NEMI, JISSO etc. (see e.g. [1]): The following challenges are of special interest for many applications:

- miniaturization (e.g. small pads and high pin count)
- high frequency (RF) capability
- improved thermal management
- move to Pb-free and halogen-free products
- low cost, especially in respect to substrates/leadframes
- system level design capability and system in package
- highly reliable interconnects

The recent introduction of the Plastic Thin Small Leadless Package (P-TSLP) has made a contribution to all of these challenges [2]. Initially the P-TSLP has been developed on the basis of wirebond interconnects. In this paper we report on the technological extension of the P-TSLP concept to flip chip interconnects. Main focus is on the investigation of the package reliability. Electrical results on first RF demonstrators up to 30 GHz have already been published elsewhere [3, 4].

During the last years, flip chip in package (FCiP) concepts have been demonstrated to be viable alternatives to flip chip on board (FCoB) technologies. Because of advantages in respect to repair a FCiP solution is often chosen instead of a FCoB solution. Leadless packages such as QFN packages matured and today they are attractive solutions especially for the RF front-end of mobile phones.

From the perspective of assembly and cost, flip chip concepts have always been competing with the well established wirebond technology. Especially the underfill process is a very unpopular and expensive assembly step. Thus, many developments in flip chip technology target alternative concepts to avoid the standard underfill dispensing process. Among others, those concepts include no flow underfills and preapplied underfills. A third approach, which we utilize in the present paper, is the concept of molding the underfill material.

For flip chip packaging, the structure of the flip chip bumps including the under bump metallization (UBM) plays a dominant role. Solder joints are generally considered to be more reliable than interconnects realized with adhesive paste or foil. If we choose a bump material which does not remelt during board level assembly, we believe we can further increase the reliability properties. In addition, the utilization of AuSn bumps offers the possibility for a low cost flux free diebond process.

The paper is organized as follows: In chapter 2, we present the assembly process flow of the leadless package. In chapter 3, we provide a description of the bumping process. In chapter 4, we present the reliability results, which fulfill even automotive requirements. In chapter 5, we show a detailed microstructure analysis of the first level interconnects. In particular, we investigated the interaction for the solder joint of the AuSn bump with the NiAu plated leadframe. First results that demonstrate also the excellent second level reliability are shown. Scanning (SEM) and transmission electron microscopy (TEM) investigations before and after stress tests show the formation of a variety of inter-metallic phases. These results are discussed within the context of their impact on reliability. In chapter 6, we highlight the excellent RF performance of the package which is enabled by the small length of electrical interconnects accounting for small parasitics. These results are discussed within the context of their impact on reliability.

2. The Assembly Process of the Leadless Package

In this section we describe the assembly concept of the flip chip package. The bumping process itself is briefly discussed in the next section. Figure 1 presents an overview on the assembly process flow of the package. We start from a rigid copper leadframe covered with mushroom shaped NiAu contacts (mainly Ni, covered with a thin Au layer for corrosion protection). The height of these NiAu pads typically amounts to 50 µm and contributes to the total height of the package (see Ref. [2]). These NiAu contacts represent the landing pads for the AuSn bumps of the flip chip. The surface of the AuSn bumps consists of an eutectic composition 80Au20Sn (melting point 280°C), which is used for creating a solder joint to the NiAu landing pads of
the Cu leadframe. The high temperature solder process above 300°C generates ternary AuSnNi intermetallics (see section 5 and Ref. [5]). After molding and laser marking, the copper strip is removed by etching leaving the chips encapsulated in a mold array. Electroless NiAu plating is applied to receive a solderable lead finish for board assembly. The mold arrays are singulated by a standard dicing process, tested and packed into tape & reel.

Prior to any discussion of reliability data or other package capabilities, a first analysis of the above process flow leads to the following statements:

- Most of the assembly processes are suitable for production on matrix level (batch processes).
- The mold process provides both underfill and package encapsulation.
- The high temperature flip chip diebond process has no need of using any fluxing agent.
- The Cu base plate does not contribute to the length of the electrical path, because it is completely removed.
- The flip chip interconnect consisting of AuSn solder will not remelt during board level assembly.
- We are dealing with a completely environmentally friendly package (lead free, halogen free, see also Ref. [6]).

Prior to the solder process, the electroplated AuSn bumps had a typical height of approx. 35 µm and the NiAu mushroom shaped contacts on the Cu leadframe had a height of 50 µm. The chip thickness was 185 µm. The whole concept has a high potential for further miniaturization, because all of the above mentioned sizes can be reduced further. For the demonstrator reported in this paper we used a package height of 0.4 mm and a package area of 1.2 x 0.8 mm².

Similar flip chip concepts have been published in Refs. [7, 8]. Ref. [7] refers to a QFN type package and high lead bumps (90Pb10Sn). Ref. [8] shows a flip chip assembly with AuSn interconnects. Both concepts however, involve the thickness of the initial Cu leadframe as electrical path between chip and the solderable areas of the package. This is in contrast to the approach presented here. Consequently, parasitic inductances and capacitances are reduced leading to superior RF performance of the P-TSLP concept.

3. **Bumping Process**

Bumps consisting of Au covered by an eutectic AuSn layer were used. A typical cross section is shown in Fig. 3. The material system AuSn has a melting temperature above the typical soldering temperatures of board level assembly. Thus, the bumps do not melt during board level assembly which improves the reliability of the solder joints. Results for the AuSn bump metallurgy can be found in Refs. [9, 10].

For the flip chip in package solution we applied the AuSn bump process which can be placed on top of an aluminum metallization as well as on top of a copper metallization. In this contribution the bumps are placed on a standard copper metallization. The last copper layer is followed by a TaN layer and a redistribution layer (RDL).
The RDL is a TiPtAu stack patterned by a lift-off process. The metallization stack is passivated by a standard PE-CVD Si₃N₄. After deposition of a TiAuTi plating layer a thick photo resist of roughly 50µm is patterned. Separate electroplating steps for Au and Sn follow. The ratio of Au to Sn is determined by an inline thickness measurement. After removal of the thick photo resist and wet etch of the plating layer the AuSn eutectic is established in a short rapid thermal anneal step at a temperature slightly above the eutectic melting temperature. This step simultaneously defines the shape of the bumps. Last step, after thinning of the wafers, is a 100% optical bump inspection (RVSI, wafer scanner 2500). The bumps are checked concerning diameter, height, shape and missing bumps.

In this contribution bumps with a height of about 35 µm and a diameter of roughly 40 µm were applied (Fig. 3). The minimum spacing of the bumps is about 40 µm.

4. Reliability Results

Packages as shown in Fig. 2b were exposed to a variety of stress tests. Conditions and results obtained on reliability tests are summarized in Tab. 1.

The TCOB stress testing program was stopped after 2200 temperature cycles. No failures were observed. Apparently the small size of the bumps does not deteriorate the reliability properties of the flip chip interconnect. During the testing program we observed neither delamination of the mold material due to thermo-mechanical stress nor insufficient adhesion of the small solder bumps to the chip. The package was shown to comply to MSL1 requirements. The bumps do not remelt inside the mold compound during board level assembly. Thus, adhesion of the bumps to the mold material persists and the formation of voids is prevented. Further improvement is achieved by the mold process which provides package encapsulation and underfill in one step. The fact that we can skip the time consuming dispensing of extra underfill material reduces the interfaces within the package and therefore increases the overall compactness of the device.

Bump shear tests were conducted using a shear speed of 0.2 mm/sec and a shear height of 10 µm. The typical shear mode was a ductile fracture in the solder material itself and therefore no reason for any reliability concern was found. The range of shear forces determined was 27 ± 5 cN.

<table>
<thead>
<tr>
<th>Test</th>
<th>Conditions</th>
<th>results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature cycling</td>
<td>Ta = -55°C to 150°C 1000 cycles</td>
<td>passed</td>
</tr>
<tr>
<td>Autoclave (AC)</td>
<td>Ta = 121°C, p=2 bar, 96h</td>
<td>passed</td>
</tr>
<tr>
<td>High humidity High</td>
<td>Ta=85°C, r.h.=85%, Uᵢ=3V, 500h</td>
<td>passed</td>
</tr>
<tr>
<td>temperature Reverse bias</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating life (OL)</td>
<td>Ta = 25°C, Iᵢ = 500 mA 1000h (0, 168, 500, E)</td>
<td>passed</td>
</tr>
<tr>
<td>Thermal shock</td>
<td>Ta = -50°C to +150°C 600 cycles, liquid to liquid</td>
<td>passed</td>
</tr>
<tr>
<td>High temperature reverse</td>
<td>Ta = 150°C, Uᵢ=3V, 500h</td>
<td>passed</td>
</tr>
<tr>
<td>Intermittent operating</td>
<td>Ta = 70°C, Tᵢ = 175°C Ton/Toff=2 min, 430h</td>
<td>passed</td>
</tr>
<tr>
<td>life (IOL)</td>
<td></td>
<td></td>
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<tr>
<td>TCoB</td>
<td>Ta=40°C to 125°C 2200 cycles (on 4-layer FR4 board )</td>
<td>passed</td>
</tr>
<tr>
<td>Bend test</td>
<td>3-point bending on 4 layer FR4 board Support distance: 90mm Amplitude : 2 mm 1000 cycles</td>
<td>passed</td>
</tr>
<tr>
<td>Ball shear</td>
<td>Shear speed 200 µm/sec Shear height 10 µm (Fracture within solder)</td>
<td>passed</td>
</tr>
<tr>
<td>MSL 1</td>
<td>260°C</td>
<td>passed</td>
</tr>
<tr>
<td>Multiple reflow</td>
<td>10 Reflow cycles (260°C) Microstructure analysis</td>
<td>passed</td>
</tr>
</tbody>
</table>

Fig. 3
Typical cross section of a AuSn bump after plating and reflow.

Table 1
Reliability test conditions as applied for the 4 pin demonstrator package P-TSLP-4-3.

The small size and low weight of small packages below the mm-range typically makes them relatively insensitive to mechanical load like drop tests or bend tests. These tests probe the quality of the board level interconnect rather than the flip chip interconnect, which is the main subject of this investigation. Extensive drop as well as bend tests were performed on the low pin count P-TSLP family without showing any problems [2]. Regarding the flip chip assemblies we limited the mechanical load tests to bend tests. In 1000 bending cycles, however, we were not able to create any failures.

5. Microstructure Analysis

In this paper we focus on the investigation of the microstructure of the first level interconnect as a function of reliability testing conditions in correlation to the electrical results. Specific attention was given to the potential risks of defect and void creation as well as to the formation of...
different inter-metallic phases. We considered especially the interfaces between the chip and the AuSn solder bump as well as the interface between solder and the internal NiAu land contact. We also show some results related to the second level interconnect referring to the interaction of the NiAu land contact with the solder of the second level interconnect for two different board metallization systems NiAu and Cu/OSP (see Fig. 4). The reliability of the package/board interconnect is not subject of this paper.

The microstructure methods comprised Scanning Electron Microscopy (SEM) combined with Energy Dispersive X-ray Analysis (EDX), Focused Ion Beam (FIB) techniques and Transmission Electron Microscopy (TEM). For SEM analysis, the samples were prepared in cross section using a mechanical procedure followed by a high-quality ion polishing finish [11]. For the TEM investigations, a FIB-based lift-off technique was applied to produce specimens oriented perpendicularly to the respective interfaces (Fig. 5) that can be directly derived from the SEM cross sections. Compared to the application of the lift off-technique for the failure analysis in Si semiconductor manufacturing, specific procedures had to be developed in order to handle the considerable differences in the ion etch rate of Sn-based solder, Si-based chip or solder and polymer-based board inside the same TEM lamella.

Figures 6 to 14 present examples for the results of the SEM/EDX investigation, which compare the microstructure in the different interfaces after 10 reflows with the reference sample (after reflow assembly to a board, but before reliability testing).

**First Level Interconnect (SEM):**

For the first level interconnect the SEM investigation revealed the existence of a well-centered Au core surrounded by a Au rich Sn containing region. In accordance to [9] the EDX results indicate that this region is formed by a \(\zeta\)-phase Au$_2$Sn intermetallic compound (IMC). Residues of the eutectic Au$_{80}$Sn$_{20}$ phase or the formation of further highly brittle IMCs such as AuSn$_4$ were not observed inside the contact. Even after 10 reflow cycles, no defect formation could be detected in the UBM and in the related interface to the Au core (see Figs. 7, 8).

For the interface with the NiAu metallization the formation of an interface layer containing Ni, Sn and Au is shown in Fig. 9. The results of the quantitative analysis are in close accordance to the results presented by Anhoeck et al [5] who suggested the formation of a ternary Ni$_3$Sn$_2$(Au) IMC with Au probably substituting part of the Ni in the lattice of the compound.
For the reference sample, the Ni₃Sn₂(Au) layer occurred in particular at the outer regions of the contact. After 10 reflows, the layer increased in thickness, homogeneously covering the whole interface (Fig. 10). Only minor void-like defects but no cracks were detected in the vicinity of the interface after stressing.

**Second Level Interconnect (SEM):**
Different results were found for the second level interconnect depending on board metallization. In case the NiAu board metallization was used, the study revealed the formation of a Ni₃Sn₂ IMC near to the Ni followed by a Ni₅Sn₆ IMC near to the solder in the interface between the (external) NiAu land surface of the package and the solder (Fig. 11).
After 10 reflows, small defects oriented perpendicularly to the interface were formed inside the Ni$_3$Sn$_2$ layer which, nevertheless, did not cause any substantial delamination (Fig. 12). Although the thickness of the Ni$_3$Sn$_4$ IMC was reduced due to starting spalling effects, a continuous IMC layer remained to protect the Ni metallization against exposure to the solder.

In comparison, using a Cu/OSP board metallization the external Ni land contact was covered by a Cu$_6$Sn$_5$ IMC (Fig. 13). After 10 reflows the thickness of the Cu$_6$Sn$_5$ IMC layer was substantially increased. Compared to the NiAu-Board metallization, the intensity of spalling was significantly less. Only few small void-like defects were found here in the interface between the electroless Ni(P) lead finish and the plated Ni metallization (Fig. 14).

**Results from TEM Investigations:**

The TEM results supported the integrity of the UBM and the interface between solder and Ni land for the first level interconnect after the thermo-mechanical stress tests (Figs. 15, 16). In addition, no defect formation near the UBM was detected and the existence of the Ni$_3$Sn$_2$(Au) IMC was confirmed using nano-spot EDX investigations.

Thus, the microstructure investigations of the specimens stressed by reflow testing showed no critical defect formations supporting the positive results of electrical tests. The excess of Au in comparison to Sn after plating leads to the formation of a Au core that covers the interface to the UBM and prevents the chip from contacts with the liquid solder during reflow [9]. Being used in the function of a spacer, this Au core accounts for a defined stand-off in between the chip and the substrate.

Furthermore, the nearly complete transformation of the eutectic Au$_{80}$Sn$_{20}$ solder into a highly temperature stable AuSn phase is a further aspect that increases the resistance of the package against reflow stressing.

Further investigations also considering the influence of thermal cycling and drop tests are in preparation.
6. High Frequency Performance of the Green Package

In addition to the general trends towards downsizing and higher functionality, also the request for high frequency capability drives package development. For first level interconnect the move to higher frequencies requires short electrical connections. Long interconnects like wirebonds act as antenna and cause significant parasitic effects, mainly caused by inductances. Wirebonds can still be used for a variety of RF applications in the 1-5 GHz region. Driven by electrical performance requirements, we observe a growing importance of flip chip interconnects with increasing frequencies.

First investigations on the electrical characterization of the P-TSLP package in flip chip version (Fig. 2) have been published in Refs. [3, 4]. These investigations demonstrate the suitability of the package concept for RF-applications up to 30 GHz. The examples investigated up to now did not yet show the frequency limit of the package (e.g. a 30 GHz frequency divider) because for these examples the used semiconductor chip was responsible for the frequency limit. With the purpose to probe the electrical limits of the package concept, investigations of our package in the range up to 100 GHz are in preparation.

7. Summary

We introduced the extension of the environmental friendly (i.e. Pb-free and halogen free) P-TSLP concept to flip chip applications using electroplated AuSn bumps. With no need of dispensing underfill or fluxing processes, the assembly flow makes the concept applicable for high volume production. The package complies to MSL1 standards and was shown to fulfill typical automotive quality requirements. The superior reliability is partly accredited to the usage of high melting AuSn bumps which do not re-melt during board level assembly. In addition, the mold process accounting for a void free underfill certainly contributes to the thermo-mechanical stability of the package. The reliability of the packaging concept was extensively investigated using different testing procedures. No electrical failures were detected during testing. With specific respect to reflow testing, the positive reliability testing results could be rationalized by the findings of a microstructure analysis study. The investigation revealed a lack of both defect initiation and extensive IMC growth even after 10 reflows particularly for the first interconnect. These results support the advantages of the technological approach based on the use of a high-melting AuSn system. For the interaction of the external NiAu land contact with the solder of the second level interconnect, the IMC growth is more significant and the formation of initial void formation and starting spalling was observed. However, these effects were found limited in size and intensity and did not develop into critical defects that define reliability risks. With respect to electrical performance, the short interconnect between chip and board makes the package very attractive for high frequency applications above 10 GHz.

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References


Novel Small Leadless Plastic Package”, International Microwave Symposium, Fort Worth, June 2004


