Announcements

Handouts - Lecture Outline and Summary
Design Problem - Answer sheet and final specs out Wed.

Review - Non-linear and active loads
Non-linear loads: large $r_{\text{eff}}$ @ large I, small V (Use biased BJT or MOSFET)
Active loads: current mirror, Lee load (Reduced common-mode gain)
Expressing gain in terms of device parameters and constraints

General Multi-stage Amplifiers - using design problem as example
Gain and bias analysis
Input and output voltage swings
Output stages: output resistance, loading on gain stage

Specialty stages
Emitter-/source-coupled pairs (diff amps)
Push-pull or Totem pole output
Cascode
Darlington
Current Source Loads: a higher maximum gain
- current source loads eliminate the compromise between voltage gain and output voltage swing

![Circuit Diagram]

Maximum Voltage gain

Bipolar: \[ |A_{v,max}| = \frac{g_m}{g_{oL} + g_{oQ}} = \frac{qI_C/kT}{I_C/V_{AL} + I_C/V_{AQ}} = \frac{V_{A,eff}}{V_{thermal}} \]

MOSFET*: \[ |A_{v,max}| = \frac{g_m}{g_{oL} + g_{oQ}} = \frac{2I_D/[V_{GS} \ V_T]}{I_D/V_{AL} + I_D/V_{AQ}} = \frac{2V_{A,eff}}{[V_{GS} \ V_T]_{\min}} \]

with \( V_{A,eff} \equiv \frac{V_{AL}V_{AQ}}{V_{AL} + V_{AQ}} \)

Typically \( V_{A,eff} >> [I \ R_L]_{\max} \)
Achieving the maximum gain: Comparing linear resistors, current sources, and active loads

MAXIMUM GAIN

<table>
<thead>
<tr>
<th>Bipolar</th>
<th>MOSFET</th>
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<tbody>
<tr>
<td>Linear resistor loads</td>
<td>$\frac{[I_C R_L]<em>{max}}{V</em>{thermal}}$, $2V_{A,eff}$</td>
</tr>
<tr>
<td>Current source loads</td>
<td>$\mu \frac{V_{thermal}}{V_{A,eff}}$, $\mu \frac{V_{thermal}}{V_{A,bias}}$</td>
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<tr>
<td>Difference mode</td>
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<tr>
<td>Active loads</td>
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<td>Common mode</td>
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Observations:
- Non-linear (current source) loads typically yield higher gain than linear resistors, i.e. $V_{A,eff} \gg [I_D R_L]_{max}$
- Bias level is not important to BJT stage gain
- A MOSFET should be biased at low level for high gain
- For active loads what increases $A_{vd}$, decreases $A_{vc}$
6.012 - Electronic Devices and Circuits

Fall 2003 Design Problem Circuit

Full schematic

- Bias chain
- Common-source gain stage with Lee load
- Source-follower stage with degeneration to provide level shift
- Common-source gain stage with current mirror load
- Emitter-follower output stage
- Push-pull output stage

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Conceptual schematic: full circuit

- **Lee load**
- **Common-source gain stage with Lee load**
- **Source-follower stage with degeneration to provide level shift**
- **Common-source gain stage with current mirror load**
- **Emitter-follower output stage**
- **Push-pull output stage**

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Fall 2003 Design Problem Analysis

Breaking out the individual stages

We'll next look at the issues associated with each stage.
Spring 2003 Design Problem Analysis

The first stage: uses the Lee Load to get large common-mode rejection in a fully-differential stage.

We find:
\[ v_{out1} = \frac{g_{o19}}{4g_{m2}} \cdot \frac{[v_{in1} + v_{in2}]}{2} + \frac{g_{m6}}{g_{o6} + 2g_{o2}} \cdot \frac{[v_{in1} v_{in2}]}{2} \]

\[ v_{out2} = \frac{g_{o19}}{4g_{m2}} \cdot \frac{[v_{in1} + v_{in2}]}{2} + \frac{g_{m6}}{g_{o6} + 2g_{o2}} \cdot \frac{[v_{in1} v_{in2}]}{2} \]

And also see:
\[ \frac{g_{o19}}{4g_{m2}} = \frac{I_{D19}}{4 \cdot 2I_{D2}}/\left[\frac{V_{SG2}}{V_{T}}\right] = \frac{[V_{SG2} V_{T}]}{2V_{A19}} \]

\[ \frac{g_{m6}}{g_{o6} + 2g_{o2}} = \frac{2I_{D6}}{I_{D6}/V_{A6} + 2I_{D2}/V_{A2}} = \frac{2V_{A6}}{\left[\frac{V_{GS6}}{V_{T}}\right]} \cdot \frac{1}{1 + V_{A6}/V_{A2}} \]

There is only so much you can do (but you can do a few things)!

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The second stage: a source-follower with degeneration to shift the level of the input to the third stage.

We find the voltage gain of this stage is:

\[ v_{\text{out}} = \frac{r_{o20}}{[r_{o20} + R_2]} \]

Hopefully this can be made close to one.

The DC level shift is:

\[ V_{\text{OUT}} = V_{\text{IN}} \begin{bmatrix} V_{GS8} & V_T \end{bmatrix} [R_2 I_{D20}] \]

Your job is to figure out why you want to shift the level, and by how much.
Fall 2003 Design Problem Analysis

The third stage:
uses the Current Mirror Load
to convert efficiently from a
double-ended to single-ended
output and to get more differ-
ential gain and common-mode
rejection.

We find:

\[
V_{\text{out}} = \frac{g_{o21}}{2g_{m10}} \frac{[V_{in1} + V_{in2}]}{2} + \frac{2g_{m13}}{g_{o13} + g_{o1} + G_{L3}} \frac{[V_{in1} V_{in2}]}{2}
\]

and:

\[
\frac{g_{o1}}{2g_{m10}} = \frac{I_{D11}/V_{A21}}{2 \cdot 2I_{D10}/[V_{SG10} V_{T}]} = \frac{[V_{SG10} V_{T}]}{2V_{A21}}
\]

\[
\frac{2g_{m13}}{g_{o13} + g_{o1} + G_{L3}} = \frac{2 \cdot 2I_{D13}/[V_{GSI3} V_{T}]}{I_{D13}/V_{A13} + I_{D11}/V_{A11} + G_{L3}} = \frac{4V_{A13}}{[V_{GSI3} V_{T}]} \cdot \frac{1}{1 + V_{A13}/V_{A11} + V_{A13} G_{L3}/I_{D11}}
\]

To maximize this gain we make \(V_{A11}\) larger and the bias current
\(I_{D13}\) large to reduce the impact of \(G_{L3}\).

What is \(G_{L3}\)? Look at Stages 4 and 5.

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Lecture 21 - Slide 9
The fourth and fifth stages:
Two parallel paths, one active when the output goes positive, the other when it goes negative. Each path consists of two emitter follower stages.

You will find that these two stages impact many aspects of your design, including:
1. The DC level at the output
2. The output voltage swing
3. The output resistance
4. The load seen by stage 3
5. The power dissipation

To begin, $Q_{16}$ and $Q_{17}$ have to be large enough to supply the current needed to $R_L$ at a modest $v_{BE}$, and the current sources $Q_{23}$ and $Q_{24}$ need to be large enough to supply the base currents $Q_{16}$ and $Q_{17}$ demand when at peak swing.
Fall 2003 Design Problem Analysis

**Output resistance:**
we begin with a single emitter follower

We have

\[
\begin{align*}
    r_{out} &= \frac{r_1 + r_t}{1 + 1} \\
    &= \frac{r_1 + r_t}{2}
\end{align*}
\]

Next look at the pair of emitter followers recognizing that the \( r_{out} \) of one is the \( r_t \) of the other:

now:

\[
\begin{align*}
    r_{out} &= \frac{r_1 + \frac{r_2 + r_t}{2 + 1}}{1 + 1} \\
        &= \frac{r_1 + \frac{r_2 + r_t}{2 + 1}}{2}
\end{align*}
\]

In the design problem we have two paths in parallel and thus have:

\[
\begin{align*}
    r_{out} &= \frac{r_{16} + r_{14}}{16 + 14} \\
            &= \frac{r_{17} + r_{15} + r_t}{17 + 15 + 16 + 14}
\end{align*}
\]

with \( r_t \equiv \frac{1}{g_{o11} + g_{o13}} \)

**Remember:** \( r = \frac{1}{g_m} = \frac{kT}{qI_C} \)

This is an important design tool.
Fall 2003 Design Problem Analysis

Load resistance on Stage 3:
again begin with a single emitter follower

We have
\[ r_{in} = r_1 + [1 + 1]R_L + r_1 + r_1 R_L \]

Next look at the pair of emitter followers recognizing that the \( r_{in} \) of one is the \( R_L \) of the other:

now:
\[ r_{in} = r_2 + [2 + 1] \{ r_1 + [1 + 1]R_L \} \]
\[ = r_2 + [2 + 1] r_1 + [2 + 1] [1 + 1]R_L \]
\[ = r_2 + 2r_1 + 1 + 2R_L \]

In the design problem we again have two paths in parallel and thus have:

\[ R_{L3} = \{ r_{14} + [14 + 1]r_{16} \} \left\| \{ r_{15} + [15 + 1]r_{17} \} + [16 + 1][14 + 1]R_L \right\} \]

Notice that some of what makes \( R_{L3} \) big, makes \( r_{out} \) big also, so compromise may be needed.
DC off-set at the output:

DC off-set:

The transfer characteristic, $V_{OUT}$ vs $v_{IN1} - v_{IN2}$, will not in general go through the origin, i.e.,

$$V_{OUT} = A_v d(v_{IN1} - v_{IN2}) + V_{OFFSET}$$

In the example in the figure $A_v d$ is $-2 \times 10^6$, and $V_{OFFSET}$ is 0.1 V.

In use (with shunt feedback, for example) the off-set with zero input is negligible. In this example, with $R = R_L$, $V_{OUT}(0)$ is only 0.1 mV.
Multi-stage amplifier analysis/design - special pair stages

**Push-pull output stages:**
High input resistance, low output resistance, large drive capability

![Diagrams of push-pull output stages](image)

- **Emitter-follower output:** negative swing imposes constraint on DC power.
- **Conventional push-pull:** limited in voltage swing by the two B-E diode drops.
- **Variation on push-pull:** larger voltage swing possible; some power cost.

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Multi-stage amplifier analysis/design - special pair stages

The Darlington connection:
A bipolar stage used to get a high input resistance

\[ r_{in} = 2 \quad r_{17} = 2 \quad \frac{2}{g_{m17}} \]

\[ r_{out} = \frac{1}{(1.5g_{o17} + g_{o15})} \]

\[ v_{out} = -\left(\frac{g_{m17}}{2}[1.5g_{o17} + g_{o15} + g_{in18}]\right) v_{in} \]

where

\[ g_{in18} = \frac{1}{\left[r_{18} + ( +1)r_{19} + ( +1)^2 R_{LOAD}\right]} \]
• **The Design Problem Circuit** - continued discussion
  
  **Gains:** expressing gain in terms of bounds on devices  
  **Output specs:** increased bias currents and larger device sizes in output stages  
  **Input/output swings:** transistors must remain active

• **General Multi-stage Amplifier Design** -  
  
  **Issues/stage choices:** matching DC levels, loading, buffering  
  **Examples:** the A 741, design problem circuit

• **Specialty stages**  
  
  **Emitter-/source-coupled pairs**  
  - our familiar differential amplifier building block  
  
  **Push-pull**  
  - large output swing with reduced quiescent power

  **Cascode**  
  - used to get large $R_{out}$; also good high freq. Performance  
  - will discuss more in Lecture 23

  **Darlington**  
  - used to get large $R_{in}$ bipolar stages