TSV Process Variations for 2.5 and 3D Semiconductor Packaging

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Topics of Discussion

- Introduction
- TSV Process Variations
- Via Ablation Processes
- Via Filling Methodologies
- Wafer Planarization and Thinning
- Wafer Joining Processes
- 3D TSV Die Stacking
- Fan Out (2.5D) Interposer Development
- Stacked Die-to-Interposer Assembly
- Summary and Conclusions

Example source: ST Micro
Introduction

• The current market driver for semiconductor package technology is to provide more functionality and improve performance without increasing package size.
• Vertically configured 3D package technology addresses this issue for a broad number of enterprise products.

Initially, the 3D package included two or more semiconductor die elements mounted on top of one another most often interconnected using wire-bond and an organic substrate interposer.
Market Drivers…

- Wireless and portable electronics continues to dominate a wide number of market segments.
- They all have a common need-
  - Greater component density
  - Expanded functionality
  - Faster operation
  - More data storage
  - Lower power
  - Longer battery life
Q-
• So, what’s driving the adoption of TSV technology?

A-
• Smaller package size-to-function ratio
• Higher operating performance
• Reduced power consumption
• Lowering semiconductor packaging cost
ITRS has defined Two TSV levels:

* International Technology Roadmap for Semiconductors

- **3D Stacked Silicon Elements**
  - Vertically joining same size homogeneous semiconductors with TSV interface.
- **2.5D Interposer Assembly**
  - TSV Interface between homogeneous and heterogeneous semiconductors using a fan-out silicon or glass based carrier.
3D TSV Packaging Market Value
2015 Forecast

Source: Yole Development
Geographic Mapping of 3D TSV Activity

Source: Yole Development
TSV Process Variations

- **Via-first** integration forms TSV holes in the basic silicon wafer prior to front-end semiconductor processing.
- **Via-middle** integration forms the small via holes in the wafer following front-end transistor formation and local interconnect processes.
- **Via-last** hole formation and plating processes are performed from the backside surface of the finished wafer.
Through Silicon Via Process

- A great deal of development has occurred in establishing an efficient and low cost method for providing a reliable interface between the top and bottom surface of the silicon based semiconductor.
- Providing very small plated or filled via holes through the contact sites initially designed for wire-bond processing is proving to be a very practical solutions.
- Advances in through-silicon-via (TSV) technology have enabled a more efficient die-to-die and die-to-substrate interface.

Example source: Invensas
TSV Implementation…

• Process related issues
  – TSV dimensions; diameter, depth, tapered or not?
  – Methodology for via ablation; plasma or laser?
  – Via fill process; copper, tungsten, PolySi, paste printing?
  – Joining method; thermo-compression, oxide fusion, adhesive, wafer-to-wafer joining, die-on-die joining, die-on wafer (2.5D) joining?
Si Via Ablation Process Variations

• Most TSV applications will be processed while the die elements remain in the wafer level format.
  – Wafer size for high volume TSV applications will range between 200mm and 300mm diameter.
  – Initial wafer thicknesses can range between 700 to 800 microns.

• There are currently two primary Si ablation processes utilized for TSV:
  – Plasma ablation (preferred)
  – Laser ablation

Example source: KEMI Silicon Inc.
Plasma Ablation
(Deep Reactive Ion Etching)

• Forming high aspect-ratio via holes are efficiently achieved using a process described as ‘inductively coupled plasma’ (ICP) ablation (this is commonly referred to as the ‘Bosch Process’).

• In preparation for the DRIE ablation processes, a dedicated system is required to apply a high-viscosity photo-resist material onto the wafers surface.
  – The coating selected must be able to withstand the aggressiveness and relatively long duration of time required for the plasma ablation process.

• The hole pattern is typically imaged and developed using a glass photo-mask stepper process or the pattern may be ablated with a numerically controlled ‘laser-direct-imaging’ (LDI) process.
• The ablation process uses plasma to progressively etch away a thin layer of the exposed silicon via sites.
• Each dry etch sequence is followed by a secondary plasma deposition that furnishes a very thin fluoro-carbon polymer passivation layer onto the via hole sidewalls.

Passivation on the sidewalls of these via features protects them from any further horizontal chemical etching.

Example source: EMC 3D
DRIE ablation cont.

• The smaller the via hole diameter the higher the speed for ablation.
  – For via diameters in the range of 10 to 25 microns, plasma will ablate the silicon material at an approximate rate of 9 microns per minute.

• In regard to the overall performance of the plasma ablation process, via wall formation is relatively smooth and uniform.

  Furthermore, with plasma ablation, all via holes on the wafer are formed simultaneously!
Laser Ablation

• The laser process is preferred by companies with low to medium volume production because-
  – It avoids the need for a number of lithographic and coating steps normally required for alternative ablation methods.
  – With laser processing, via locations, diameter, shape and depth can be digitally programmed.
• This factor simplifies TSV implementation by enabling faster setup and product changeover.
The actual ablation rate is determined by the laser repetition rate and the speed at which individual via holes can be formed:

- The number of laser pulses and the pulse energy dictate via depth while the beams size governs via diameter.
- Overall, the short-pulse laser process is said to produce a 10 micron diameter via hole.

These systems can operate at what is considered a very high speed for laser ablation in silicon:

- Up to 10,000 via sites per second (depending on the via hole diameter and depth).
Laser or Plasma?

• Selecting which TSV ablation process will depend a great deal on economics and throughput criteria.

• Laser systems developed for via hole ablation, although relatively slower than chemical ablation, are numerically controlled, requiring little, if any, complex tooling or masking operations.

• Because plasma via ablation has a higher throughput it is currently favored by those involved with high volume TSV applications.

With either process, via holes are commonly ablated from the active side of the wafer to a depth that is slightly less than the overall thickness of the silicon material.
Hole Formation Capability for Via First and Via Middle Process

• Although 5 to 10um diameter TSVs are most common for via-first and via middle ablation, experts believe the plasma ablation process has the potential for furnishing significantly smaller hole features.

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<tbody>
<tr>
<td>Minimum TSV pitch (um)</td>
<td>3.8</td>
<td>3.6</td>
<td>3.4</td>
<td>3.3</td>
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<tr>
<td>Minimum TSV diameter (um)</td>
<td>1.9</td>
<td>1.8</td>
<td>1.7</td>
<td>1.6</td>
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<tr>
<td>Maximum TSV aspect ratio (L/D)</td>
<td>12</td>
<td>14</td>
<td>16</td>
<td>18</td>
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Source: International Technology Roadmap for Semiconductors,
Via Filling

• Although conductive polymers can be used for via filling, a majority of TSV users have adopted a copper plating process to fill the tiny vias---

1. A thin titanium adhesion layer is first applied to the wafers surface and TSV features using sputtering process.
2. Physical Vapor Deposition (PVD) is then applied to provide a conformal low resistivity Cu seed layer.
3. Electroplating is finally performed using a copper sulfamate or other Cu plating solution.
TSV forming, plating and wafer thinning sequence

1- Apply photo resist and image

2- Ablate via features, remove photo resist

3- Sputter coat and deposit seed layer

4- Electroplate Cu to fill via

The copper electro-plating via filling process is complete in a relatively short time leaving a thin Cu layer (~5 micron) over the active surface of the wafer.
Domestic TSV Foundry Example
ALLVIA, Sunnyvale, California

Dry plasma etch capability –
• Via diameters as small as 10 um with depths as great as 500um.
• Capability to open blind vias from the front or backside of a wafer.
• Deposition process provides void free solid copper filled vias.
• Silicon can be removed from the wafers backside to provide a Cu post*
  extension.

*Typical via post extensions: 50 um, 75 um, or 100 um.
Wafer Planarization and Thinning

Because of its higher thinning rate, mechanical grinding is currently the most common technique used for the primary wafer thinning step.

- There are four primary methods available for wafer thinning:
  1. Chemical-mechanical polishing
  2. Wet etching (plasma)
  3. Dry chemical etching
  4. Mechanical grinding

Example source: Strasbaugh Corp
The principal wafer-to-wafer bonding methodologies currently being used for 3D TSV interconnects are:

1) fusion (or molecular) bonding
2) metal-metal thermo-compression bonding
3) adhesion bonding

There are also alternative joining variations that may employ conductive polymer bonding and oxide bonding processes.

Each of these methods have their advantages and disadvantages but there is really no standard process for TSV wafer preparation and joining.
1. Fusion Bonding

- This joining process is a two stage procedure that begins with the initial precise alignment and a room temperature pre-bonding of the wafers.
- Following pre-bond, the wafer is exposed to an annealing process that includes high temperature and pressure.
- This joining process is significantly enhanced with the deposition of a thin layer of tin-alloy onto the exposed copper TSV features.
2. Thermo-compression Bonding

- The direct Cu-to-Cu bonding process is preferred by many in the industry for TSV joining because the process simultaneously forms both a mechanical and electrical connection between wafer layers.

The bonding process requires very high temperature, high pressure, and a relatively long time under heat and pressure to complete the joining process.

Example source: Microsystems Technology Laboratories, MIT
3. Adhesion Bonding

- Adhesion materials are an anisotropic conductive adhesive that provides both mechanical strength and electrical conductivity at TSV interconnection points.
- The materials can be spin or spray coated onto the silicon wafers or applied as a film media and bonded at a moderate 250°C.
- **The advantages of adhesion bonding** - reduced space between wafers, requires lower assembly process temperatures and it has the potential to reduce cost.
- **Disadvantage of conductive adhesives** - an additional passivation (dielectric coating) may be required to insulate the backside surface of the wafers.
Process Control Concerns

• There are a number of key process controls that will require close monitoring:
  – Wafer-to-wafer alignment required for the fusion metal process is +/- 150nm.
  – Metal oxide, if allowed to form, can prevent adequate bond formation
  – Excessive heat and bonding force can result in non uniform bond strength between the wafer layers.

For either Cu-to-Cu process variations, control of surface roughness and oxidation is important to allow the apposing metal surfaces to come into intimate contact.
3D TSV Die Stacking

- Many package assembly service providers have independently developed proprietary processes for TSV.
- Memory semiconductors in particular, are ideal for direct vertical TSV joining because many of the I/O (pins) can be connected in parallel.

4Gb DRAM, 512Mb x 8die stack

Example source: Mitsubishi
3D TSV Implementation Issues

- Due to the process complexities and semiconductor yield concerns associated with wafer-to-wafer joining, many companies are stacking individual die elements.
- Even though wafer fabrication processes for memory has a relatively high yield, the pretesting of individual die elements before joining ensures that every die within the stack are ‘known good’.

*Illustration source: Yole Development*
Implementation Issues cont.

- **Cost Issues**
  - Equipment throughput, facility development, tooling costs, amortization period.
  - Associated consumables; gasses, slurries, resist materials.
  - Fab parameters; number of wafers, engineering resources.
  - Geographic local; operator costs, environmental restrictions.

*Clean room photo source: EV Group*
Fan-out 2.5D Interposer Development

• If the die outline cannot provide the surface area to accommodate a suitable contact array for SMT assembly, the fan-out silicon based interposer may become necessary.

• One process developed for the silicon based fan-out interposers first applies a polyimide passivation coating onto a bare wafer.

• To enable the copper filling of the TSV features and the redistribution of the TSV sites to a wider spaced contact pattern, the wafer is subjected to a series of metallization processes.
2.5D Silicon Interposer with TSV and RDL

- The Si interposer acts as an intermediate carrier for interconnecting high pin count and 3D configured devices:
  - Multiple processor interface
  - Interfacing processor(s) and memory between heterogeneous die elements
  - Between stacked 3D Si-system and an organic substrate

Example source: Fraunhofer IZM
2.5D Memory and Logic Assembly

- Samsung and Micron formed a consortium to develop a serial specification for a memory technology called the ‘Hybrid Memory Cube’ (HMC).
- HMC will incorporate DRAM arrays stacked on a logic chip.
- Targeted for late 2013 or early 2014.

The product will be initially aimed for networking systems and high-end servers.

*Example source: Micron Technology*
Summary and Conclusions:

• The major challenge for today’s electronic products is the control of overall system costs and reducing power consumption.

• 3D TSV technology is seen to hold an attractive solution, however, the technology currently remains hostage to a very limited homogeneous family of products.

• 2.5D TSV on the other hand, provides the platform for combining a broad combination of heterogeneous semiconductor elements with a single package outline.

• Companies will need to make some critical monetary decisions on whether TSV capability remains within the semiconductor foundry or is outsourced to specialists focusing on TSV technologies.
Semiconductor Yield Concerns

• Due to the process complexities and semiconductor yield concerns associated with wafer-to-wafer joining, many companies are stacking individual die elements.

• Key concerns-
  – Wafer level test; 50%?, 75%?, 100%?
  – Wafer level process yield; 85%?, 95%?, 97%?
  – Damage during singulation; chips, cracks

• Although wafer level testing is gaining acceptance, the most efficient and thorough electrical testing has traditionally relied on the singulated die.
TSV Standards Activity...

Design Enablement Standard Committee: Si2, JEDEC
   Focus Area: EDA, Chip to Chip interface
Standard Committee: SEMI, Sematech, GSA
   Focus Area: Manufacturing process, equipment & material.
SiP integration & Test Standard Committee: SEMI, Sematech, GSA, JEDEC
   Focus Area: Supply chain, shipping method, wafer support system, incoming/outgoing specs, KGD strategy & test hardware.
Reliability Assurance Standard Committee: JEDEC
   Focus Area: Lifetime/reliability criteria, thermal & thermal-mechanical attributes.
Key factor...reducing risk

After considering other flows to form TSV through active silicon, most companies have settled on only two:

- **Via-Middle**, Before thinning the finished wafer, ablate and fill vias from topside.
- **Via-Last**, While temporarily bonded to carriers, ablate and fill vias from the backside.

Thank you

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