Traditionally, developers designing control applications with communications capabilities have had to make compromises in their designs. Real-time control requires a microcontroller with complex mathematical capabilities, a pipeline designed to facilitate accurate control loop processing, and an internal architecture that guarantees deterministic control and peripheral responsiveness. Efficient communications, on the other hand, is well-suited to the decision-based architecture of more general-purpose processors.

For the most cost-effective design, developers often use a single device to implement both control and communications functionality. However, this allows developers to optimize only one part of the system based on which kind of processor is selected. If a real-time control microcontroller is chosen, for example, the real-time control loop can be designed with optimal performance and efficiency. However, the communications link will suffer in terms of bandwidth or responsiveness as it will be serviced with secondary priority compared to the control loop. Consider a programmable logic controller serving as the central intelligence in an industrial automation application which directs multiple motors over an Ethernet link. Latency over the communications interface, then, becomes critical to accuracy. In addition, if the microcontroller does not have the processing capacity to reliably handle the connection technology of choice under worst-case operating conditions, developers may be forced to use a different, less than ideal interface.

On the other hand, if a communications microcontroller is selected as the core of the system, the communications link will have high reliability and throughput. However, this will come at the expense of compromising control reliability, accuracy, and efficiency since an applications processor does not have the robust interrupt infrastructure of a real-time control microcontroller. Developers will also not have the advanced computational capabilities or real-time peripherals necessary to implement custom IP to improve control-loop performance such as enhanced filtering or proprietary vibration analysis. They will also lack other integrated functionality such as power factor correction (PFC).

In addition to these issues, implementing real-time control and communications on the same device introduces significant software complexity, regardless of whether a microcontroller or...
applications processor is used. Communications, diagnostics and housekeeping tasks all compete with the control loop for processor cycles, making it extremely challenging to guarantee real-time responsiveness for control and communications simultaneously. Developers also have to manage other shared resources such as memory and access to peripherals. Mechanisms to mitigate and resolve conflict add further complexity and latency to the system.

Developers can resolve performance and real-time responsiveness issues by specifying a higher performance device, but only at the expense of correspondingly higher system cost. Alternatively, developers can avoid many of these compromises by using a separate processor for the control loop and another for managing communications and system housekeeping tasks. This approach, while meeting performance and reliability requirements, significantly impacts system cost through increased board size and component cost. Hardware design complexity increases as well, as does communication latency between the processors. Ideally, engineers need an architecture where all of these compromises and tradeoffs can be avoided.

Enter C2000™ Concerto™ microcontrollers.

TI's new Concerto microcontrollers utilize a dual subsystem architecture comprised of a TI C28x core and ARM® Cortex™-M3 core. This hybrid architecture combines the industry’s best technologies for control and host communications functionality into a single controller that provides the performance, efficiency, and reliability required to maintain real-time control loops with the fast responsiveness required for low-latency communications.

TI developed the Concerto platform to eliminate the compromises engineers have to make when designing systems needing real-time control and communications capabilities. The ARM Cortex-M3 architecture is used...
widely throughout the industry for host communications and has a large ecosystem of tools and software. Cortex-M3 is also well-established as a proven platform for developing advanced human-machine interfaces (HMI) and graphical user interfaces (GUI).

Similarly, the C28x core is the industry’s leading platform for control applications of all types. The C28x architecture has been optimized to efficiently and reliably manage complex control algorithms with its integrated floating-point processor and streamlined memory architecture that exceeds the capabilities of more general-purpose cores. It also offers best-in-class control peripherals to provide the highest efficiency, accuracy, and performance.

With Concerto MCUs, TI has leveraged two proven architectures to create tailored solutions for a diverse range of control applications (see Figure 1). Functionality is cleanly partitioned between cores, greatly simplifying design and increasing system reliability by eliminating contention for shared resources between real-time control tasks and communication drivers.

The Concerto platform offers an extensive variety of options so that developers can select a processor with the ideal allocation of resources to match a wide range of applications. The entry-level Concerto MCU, available for under $7, offers 60 MHz for control (C28x) and 60 MHz for communications (Cortex-M3). Mid-level Concerto microcontrollers provide 75 MHz for control and 75 MHz for communications. For advanced applications, high-end Concerto devices offer up to 150 MHz for control and 125 MHz for communications.

In terms of memory, Concerto dual-subsystem microcontrollers offer both flexible RAM and Flash configurations. RAM configurations are available up to a total of 232KB shared between the device cores. In addition, up to 1.5MB of Flash and 4KB of messaging RAM is also available on various configurations of the device.

Figure 1. Concerto 32-bit microcontrollers combine TI’s class-leading-performance C28x core and control peripherals with an ARM Cortex-M3 core and connectivity peripherals to deliver a clearly partitioned architecture that supports real-time control and advanced connectivity in a single, cost-efficient device.
The messaging RAM provides an efficient and fast mechanism for passing messages between cores, and a method for time-stamping is provided to enable synchronization when necessary. Each core can write to its own messaging RAM and then signal the other core that data is ready for reading. With no tokens, locks, or semaphores to manage, the cores can communicate reliably with minimal latency. TI understands the importance of simple communication between cores and also provides a complete inter-processor communication library with efficient protocols to further streamline messaging.

Concerto dual-system controllers bring together all of the control and communications peripherals required for a wide range of applications (see Table 1). The control peripherals of the Concerto architecture are based on the industry-leading peripherals that help define C2000 MCUs. The integrated Pulse Width Modulators (PWM) are the best in the industry, offering ~150 picosecond resolution per channel for the highest control precision. Additionally, Concerto MCUs offer a flexible, multi-instantiated PWM module with multiple compare events and the built-in support required for high-frequency power control, such as shadowed registers, adjustable dead-band, and programmable cycle-by-cycle or one-shot fault handling.

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<tr>
<th>Control Peripherals</th>
<th>Communication Peripherals</th>
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<tr>
<td>Enhanced PWMs with ~100 picosecond resolution</td>
<td>10/100 Ethernet MAC with 1588 (optional)</td>
</tr>
<tr>
<td>Two 12-bit, 2.9 MSPS ADCs, each with 2 S/H, up to 24 total channels</td>
<td>USB 2.0 OTG with integrated PHY (optional)</td>
</tr>
<tr>
<td>Analog comparators with internal DAC reference</td>
<td>Dual CAN</td>
</tr>
<tr>
<td></td>
<td>Multiple SPI, UART, I²C</td>
</tr>
<tr>
<td></td>
<td>8-/16-/32-bit External Memory Interface</td>
</tr>
</tbody>
</table>

Table 1. Integrated peripherals. Concerto dual-subsystem controllers bring together all of the control and communications peripherals required for a wide range of applications.

Further improving performance and accuracy are two independent dual sample and hold ADCs operating at up to 2.9 Msamples/second each. To simplify design, all inputs to the ADCs are routed through a common input, and which ADC actually handles a signal is managed in software by the driver. In this way, developers are able to focus on the inputs themselves instead of having to worry about which ADC a signal is allocated. Each ADC can also sample and hold (S/H) two values, together enabling four measurements to be taken simultaneously. The ability to synchronize samples is critical for robust control systems. Many compensation algorithms require pairs of current and/or voltage measurements. Rather than sampling the current, processing it, and then sampling the voltage at a different time, both current and voltage can be measured simultaneously to ensure maximum accuracy.

Completing the signal chain are asynchronous analog comparators which offer superior performance compared to the digital comparators that the majority of MCUs have integrated. Rather than have to wait for the next clock cycle to trigger on an over-or-under current condition, Concerto MCUs can trip immediately. Developers also have the flexibility to configure the trip threshold through the use of a reference voltage.
Signal accuracy is maintained at the architectural level as well. Many of the signals running through the Concerto peripherals, especially the communication interfaces, can operate at high frequencies. The Concerto architecture has been specifically designed to minimize electromagnetic interference (EMI) between the various high frequency control and communication signals being managed to ensure the most accurate and reliable system operation.

Traditionally, multi-core architectures share many system resources, which introduces a variety of challenging sharing and contention issues. Allocation of resources such as peripherals adds a layer of complexity since the cores have to manage ownership of shared resources using complex mechanisms that attempt to minimize the effects of contention and latency. Even with such mechanisms, access to peripherals can be delayed, thereby reducing signaling accuracy and negatively impacting real-time responsiveness.

The Concerto architecture eliminates the need for complex sharing and contention mechanisms by implementing the C28x and Cortex-M3 cores as independent subsystems. As a result, each core is complete with its own interrupt controller, memory, and dedicated peripherals appropriate to the tasks the core is expected to handle. In addition, C28x control peripherals are not directly accessible by the Cortex-M3 core, nor are the various Cortex-M3 communication peripherals accessible by the C28x core. In this way, the host processor cannot interfere with real-time control processes, nor can the control side of the system impact any communication interfaces.

This partitioning of the Concerto architecture both increases system reliability and greatly simplifies application development. Because each core manages its own peripherals, developers can ensure that code on the other core cannot impair system performance or the system’s ability to meet real-time deadlines. In addition, software libraries can be used without modification. For example, when library code for real-time control algorithms and communication stacks are executed on the same core, developers have to analyze and verify that the maximum latency of functions from each library is within the interrupt responsiveness limitations of the other library. By executing code from each library on separate cores, no such analysis or code modification is required.

The independence of each of the cores extends even to clock and power management. When control and communications code are implemented on the same core, these functions are effectively tied together because if either function requires the clock to run at full frequency, the entire processor is clocked at this frequency.

With the Concerto dual-subsystem architecture, even though the two cores share the same clock source, each can be clocked at a different frequency, depending upon the application. This ability to dynamically adjust the operating frequency for each core separately results in substantial power savings. Consider a motor drive system with an Ethernet. When the system is not actively transmitting, it can dynamically drop the clock frequency of the Cortex-M3 to a level that allows the processor to recognize incoming data while still...
clocking at the full frequency of the C28x to operate the motor. Similarly, if the motor is turned off but data is being received at full bandwidth, the Cortex-M3 can be clocked at full frequency while the C28x clock frequency is dropped.

The dual subsystem architecture of Concerto microcontrollers also accelerates system design compared to both single-core and separate control/communications approaches. While code development for the Cortex-M3 and C28x cores is completely segregated, programming is done within the shared integrated development environment (IDE) of TI's industry-leading Code Composer Studio™. Rather than creating a whole new architecture that requires developers to learn a different set of tools and libraries, Concerto microcontrollers merge the powerful and existing development infrastructure of the ARM Cortex-M3 and C2000 platforms. Each processor is treated as a separate thread within Code Composer Studio IDE, and developers can debug both cores simultaneously as well as monitor and trigger trace events on communications between the cores.

Given that control and communications are entirely different functions, each core has its own software libraries and application tools. All Concerto software, documentation, training and support can be found in the controlSUITE™ platform as shown in Figure 3 on the following page.

On the control side, controlSUITE software allows developers to work at a high level to design and optimize control-loop software to achieve the level of precision and accuracy required for the application. For developers new to control applications, controlSUITE includes libraries for motor control and digital power conversion. Libraries include advanced processing functions such as power factor correction (PFC), filtering, and diagnostics that enhance system value while allowing developers to differentiate their systems from the competition. In addition, the libraries include many useful system management functions such as support for in-system programming and software to facilitate IEC 60730 certification.
On the communications side, TI offers development tools such as plcSUITE™ to accelerate the design of robust communications interfaces by enabling developers to quickly build all of the software and drivers required to manage real-time links. In the controlSUITE platform, developers can also leverage a wealth of turnkey communications software for a variety of interfaces, including Ethernet, CAN, SPI, USB, USB On-the-Go (OTG), and IEEE 1588. Developers can also create intuitive human-machine interfaces (HMI) using extensive graphics libraries in the controlSUITE platform. TI also offers the Concerto F28M35x Experimenter’s Kit which allows developers to test the capabilities of Concerto controllers just minutes after taking it out of the box.

This approach to development allows developers to leverage their existing software base to both reduce code development investment and speed time-to-market. Application code written for TI’s C2000 devices all port seamlessly to Concerto dual-core microcontrollers. In addition, developers can rely upon the extensive ARM ecosystem built around the Cortex-M3 for application-specific code libraries and design tools.

Safety

One exception to the dedicated peripheral partitioning is the shared use of the two integrated ADCs. Both cores have access to the ADC result registers to allow for independent usage of the ADCs in control,
communication, and/or system diagnostics. For example, one ADC can serve as a sense feedback for two motors while the other ADC can be dedicated to host purposes such as temperature sensing and a communications link.

For those applications requiring advanced safety features, the shared nature of the ADC can be used as a safety and reliability mechanism. In this configuration, the ADC is controlled by the C28x core but can be monitored by the Cortex-M3 core. In effect, this allows the Cortex-M3 to serve as a supervisory core to the real-time control subsystem, providing an integrated means for ensuring that the C28x is performing as expected.

The Concerto architecture has been designed with a number of other safety enhancements:

- **Built-in clock backup**: If the clock source for a Concerto controller fails, an internal 10-MHz clock is activated to keep the system alive. It can allow for a graceful shutdown.
- **Self-check**: Because the Concerto architecture is comprised of two independent controllers, they can dynamically confirm reliable runtime operation of each other.
- **Self-test**: The self-test capabilities of Concerto controllers include memory and logic testing. In addition, the integrated ADCs can calibrate and test themselves to reduce manufacturing and system calibration complexity.
- **Memory reliability**: Data stored in memory is verified using either error code correction (ECC) or parity checks, both implemented in hardware. ECC offers one-bit error correction and two-bit error detection to ensure reliable system operation.

Concerto changes the way developers design embedded systems. Rather than have to choose between compromising real-time control responsiveness or communications reliability, developers can guarantee best-in-class performance for both control and communications functions. With the Concerto MCU's dual-subsystem architecture, partitioning is easy, thus simplifying system design and speeding time to market. Developers can leverage their existing IP from C2000-based designs into a single Concerto controller to reduce cost without compromising reliability or performance. In addition, the enhanced safety features of the Concerto architecture allow developers to add more safety and security to a wide range of applications. As a result, developers no longer have to choose between optimizing connectivity and real-time control.

For more information on starting your next design with Concerto MCUs, visit [www.ti.com/concerto](http://www.ti.com/concerto).
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