Ultra Thin 3D eWLB-PoP (embedded Wafer Level Ball Grid Array - Package on Package) Technology

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Package-on-Package (PoP)
Mobile Trends - Smartphone and Tablet

- Market size projections are dynamic & other reports suggest larger TAM - more from Smartphone

Smartphones are the major market for PoP
PoP Drivers and Limitations

Drivers
- Form-factor Reduction (Vertical Integration of Memory & bottom PoP (Logic) Package >> less than 1mm PoP
- Performance Gain (BW) required with High-Speed DDR

Limitations/Challenges
- Max die size limitation due to the presence of top lands & UF design rules
- Thermal constraints due to the unidirectional thermal path - mainly through the substrate & PCB

-90% of heat removed from Bottom PoP through conduction into PCB
eWLB : Form Factor, Performance and Integration

Superior Solutions spanning the needs of mobile and other high-performance applications

- MCP configurations (thickness down to 0.5mm)
- The thinnest 3D solution (Stack thickness down to 0.8mm)
- Scalable carrier size with heterogeneous integration platform
- Leading cost/performance solutions (co-design optimized)
- Ultra fine ball pitch (down to 0.3mm) and maximum I/O density
- Excellent electrical and thermal performance
- Enhanced reliability with advanced dielectric materials
- 3D-PoP configurations - both single and double sided
eWLB Products Portfolio

2D
- Single chip eWLB
- Multi-chip eWLB
- eWLL
- 2.5D / Extended eWLB

2.5D
- Flipchip eWLB

3D
- 3D eWLB
- eWLB-PoP

package or die
Ultra Low Profile PoP Solution: 
**eWLB-PoP (embedded Wafer level PoP)**

- Successfully qualified for CLR & BLR of 14x14mm eWLB-PoP
- Thin POP (250um pkg body thickness)
- Sub mm (<1.0mm) PoP height
- Low warpage during solder reflow cycles
- Compatible with ELK (28nm)
- Good thermal performance
eWLB-PoP Key Features

• PoP is a rapidly growing package type targeted to the mobile communications market for Smart phones and Tablets
  • POP packaging is expected to push performance and form factor favoring technology <1.0mm thick sharing same AP ICs.

• eWLB-PoP provides a ultra low height and small form factor PoP solution due to the thin form factor and reduced warpage base package
  • No substrate - thinner and less mismatch to PCB
  • Wafer level processing - an inline/batch process and cost-effective solutions with larger carrier.

• Cost-effective high volume manufacturable technology with over 3-yr production experiences.
eWLB-PoP Assembly Process Flow

1S Thin eWLB Process

3D vertical Interconnection

Laser Ablation

Clean, Top Ball Attach, Reflow, Clean

PKG Saw

AOI
eWLB-PoP Bottom Package Cross-Sections
eWLB-PoP

PKG height = 0.5mm (including solder balls)

14x14mm  12x12mm  10x10mm
8x8mm die  8x8mm die  8x8mm die
0.5mm TBP  0.4mm TBP  0.4mm TBP
0.4mm BBP  0.4mm BBP  0.4mm BBP
eWLB Top package SMT mounting (Without Board Level Underfill)
eWLB-PoP (10x10mm) Cross-Sections

Paxkage h=0.77mm
eWLB-PoP (14x14mm) Cross-sections

**Sub mm package height PoP**

- Die Stacked Memory
- AP eWLB-PoP
- Top Memory PKG
- eWLB-PoP Bottom PKG
- PCB Substrate

~ 0.9 mm
eWLB-PoP Component-level Reliability

<table>
<thead>
<tr>
<th>Reliability Test</th>
<th>JEDEC</th>
<th>Test Condition</th>
<th>Read-out</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSL1 + 3x reflows</td>
<td>JESD20-A120</td>
<td>85°C / 85% RH</td>
<td>168hrs</td>
<td>Pass</td>
</tr>
<tr>
<td>Unbiased HAST (W/ MSL1)</td>
<td>JESD22-A118</td>
<td>130°C, 85%RH</td>
<td>168hrs</td>
<td>Pass</td>
</tr>
<tr>
<td>Temperature Cycling (TC-B, w/MSL1)</td>
<td>JESD22-A104</td>
<td>-55°C/125°C; 2Cy/hr</td>
<td>1000x</td>
<td>Pass</td>
</tr>
<tr>
<td>High Temp. Storage (HTS w/o PC)</td>
<td>JESD22-A103</td>
<td>150°C</td>
<td>1000hr</td>
<td>Pass</td>
</tr>
</tbody>
</table>

eWLB-PoP Board-level Reliability

- **JEDEC Drop Test**
  - First Failure @ 161 drops without underfill (10x10mm)
  - First Failure @ 98 drops without underfill (14x14mm)

- **JEDEC TCoB (-40/125C; 8 layer board)**
  - First Failure after 1000 cycles without underfill (10x10mm) → JEDEC std board.
  - First Failure after 2000 cycles without underfill (14x14mm) → customer designed board
10x10mm eWLB-PoP Board Level Test - without underfill

First Failure @1091x

First failure after 150 drops
14x14mm eWLB-PoP Board Level Test - without underfill

**TCoB first failure after 2000 cycles**

**First failure after 98 drops**
eWLB Electrical Characterization

Plot of electrical parasitic values of RLC of fcBGA and eWLB @ 1GHz.

eWLB has 68% less in resistance, 66% less in inductance and 39% less capacitance compared to fcBGA. It is mainly due to shorter interconnection in eWLB.
4L Laminate and 2L eWLB
(design examples for same functions)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Laminate</th>
<th>eWLB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pad Pitch</td>
<td>40um staggered (80um in one row)</td>
<td>40um staggered (80um in one row)</td>
</tr>
<tr>
<td>Signal Trace W/S</td>
<td>30um/30um</td>
<td>10um/10um</td>
</tr>
<tr>
<td>Via Diameter</td>
<td>60um/100 um (in prepage/core)</td>
<td>30um</td>
</tr>
<tr>
<td>Capture Pad</td>
<td>130um/200um</td>
<td>60um</td>
</tr>
<tr>
<td>Via Pad Clearance</td>
<td>50um</td>
<td>10um</td>
</tr>
</tbody>
</table>

- Finer L/S in eWLB allows to implement signal traces in smaller area, to allocate more area for P/G nets.
- Via and via pad are 2-3 times smaller in eWLB.
- Typically 2-3 times area saving can be made using eWLB routing. This translates to have 2-3 times less layers to implement the same nets with the same package size.
Power/Ground Impedance Comparison

<table>
<thead>
<tr>
<th>net</th>
<th>Inductance (nH)</th>
<th>Resistance (mΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2-layer eWLB</td>
<td>4-layer laminate</td>
</tr>
<tr>
<td>1</td>
<td>0.43</td>
<td>1.77</td>
</tr>
<tr>
<td>2</td>
<td>0.24</td>
<td>2.03</td>
</tr>
<tr>
<td>3</td>
<td>0.57</td>
<td>1.51</td>
</tr>
<tr>
<td>4</td>
<td>0.25</td>
<td>1.08</td>
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</table>

- Comparison is made on two actual designs.
- Impedance (R and L) comparisons are shown for identical P/G connections at the IC for the two technologies.
- Lower inductance (L) and resistance (R) for eWLB is mainly due to larger areas/patterns implemented for P/G nets.
This simulation extracts a portion of a large package to model the behavior of one of the memory buses in an eWLB-PoP.
• The above simulated eye diagrams show excellent signal integrity. These results include simultaneous switching noise and crosstalk for the 10-channel bus.
• Higher power-plane capacitance (for decoupling purpose) than in laminate design, which would help to yield a better power integrity performance from eWLB-PoP
• Verified functionality with live device used in production for Dual Core AP device.
Thermal simulation data of 14x14mm PoPb (eWLB & fcPoP) comparison

<table>
<thead>
<tr>
<th>Package</th>
<th>Power (W)</th>
<th>$T_A$ (°C)</th>
<th>$T_J$ (°C)</th>
<th>$\Theta_{JA}$ (°C/W)</th>
<th>$\Psi_{JT}$ (°C/W)</th>
<th>$\Psi_{JB}$ (°C/W)</th>
<th>$\Theta_{JB}$ (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>eWLB-POP 14x14mm</td>
<td>3</td>
<td>50.0</td>
<td>103.1</td>
<td>17.7</td>
<td>0.01</td>
<td>5.22</td>
<td>5.61</td>
</tr>
<tr>
<td>fcPoPb 14x14mm</td>
<td>3</td>
<td>50.0</td>
<td>103.6</td>
<td>17.85</td>
<td>0.05</td>
<td>5.89</td>
<td>6.20</td>
</tr>
</tbody>
</table>

Fig. 1. eWLB version under natural convection and 3W.

Fig. 2: fcPoPb version under natural convection and 3W.
Normalized Thermo-Moire Warpage Behavior with package types

Normalized warpage over package height: low eWLB-PoP showed quite good warpage behavior.
Ultra thin eWLB-PoP warpage is controllable within +/- 60um.
Summary

1. Ultra low profile eWLB-PoP was developed using eWLB (fanout WLP) and MLP technology of laser ablation and solder filling.

2. Less than 1mm PoP height with Std stacked memory

3. Passed JEDEC standard component and board level reliability tests.

4. eWLB-PoP showed good electrical and thermal performance.

5. eWLB-PoP has low warpage than other thin packages.

6. eWLB-PoP technology provides more value-add in performance and promises to be a new packaging platform that can expand its application range to various types of mobile/portable devices as well as 3D SiP systems.
Thanks so much for your attention

谢谢。
Salamat sa inyo.
மன்னி.
감사합니다.