The SST39SF010A / SST39SF020A / SST39SF040 are CMOS Multi-Purpose Flash (MPF) devices manufactured with SST proprietary, high performance CMOS SuperFlash technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39SF010A / SST39SF020A / SST39SF040 write (Program or Erase) with a 4.5-5.5V power supply, and conforms to JEDEC standard pinouts for x8 memories.

Features

- **Organized as 128K x8 / 256K x8 / 512K x8**
- **Single 4.5-5.5V Read and Write Operations**
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption**
  (typical values at 14 MHz)
  - Active Current: 10 mA (typical)
  - Standby Current: 30 µA (typical)
- **Sector-Erase Capability**
  - Uniform 4 KByte sectors
- **Fast Read Access Time:**
  - 55 ns
  - 70 ns
- **Latched Address and Data**
- **Automatic Write Timing**
  - Internal VPP Generation
- **Fast Erase and Byte-Program**
  - Sector-Erase Time: 18 ms (typical)
  - Chip-Erase Time: 70 ms (typical)
  - Byte-Program Time: 14 µs (typical)
  - Chip Rewrite Time:
    - 2 seconds (typical) for SST39SF010A
    - 4 seconds (typical) for SST39SF020A
    - 8 seconds (typical) for SST39SF040
- **End-of-Write Detection**
  - Toggle Bit
  - Data# Polling
- **TTL I/O Compatibility**
- **JEDEC Standard**
  - Flash EEPROM Pinouts and command sets
- **Packages Available**
  - 32-lead PLCC
  - 32-lead TSOP (8mm x 14mm)
  - 32-pin PDIP
- **All devices are RoHS compliant**

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  - Toggle Bit
  - Data# Polling
- **TTL I/O Compatibility**
- **JEDEC Standard**
  - Flash EEPROM Pinouts and command sets
- **Packages Available**
  - 32-lead PLCC
  - 32-lead TSOP (8mm x 14mm)
  - 32-pin PDIP
- **All devices are RoHS compliant**
Product Description

The SST39SF010A/020A/040 are CMOS Multi-Purpose Flash (MPF) manufactured with SST’s proprietary, high performance CMOS SuperFlash technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39SF010A/020A/040 devices write (Program or Erase) with a 4.5-5.5V power supply. The SST39SF010A/020A/040 devices conform to JEDEC standard pinouts for x8 memories.

Featuring high performance Byte-Program, the SST39SF010A/020A/040 devices provide a maximum Byte-Program time of 20 µsec. These devices use Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent write, they have on-chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with a guaranteed typical endurance of 100,000 cycles. Data retention is rated at greater than 100 years.

The SST39SF010A/020A/040 devices are suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, they significantly improve performance and reliability, while lowering power consumption. They inherently use less energy during erase and program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. These devices also improve flexibility while lowering the cost for program, data, and configuration storage applications.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

To meet high density, surface mount requirements, the SST39SF010A/020A/040 are offered in 32-lead PLCC and 32-lead TSOP packages. A 600 mil, 32-pin PDIP is also available. See Figures 2, 3, and 4 for pin assignments.
Block Diagram

Figure 1: Functional Block Diagram
Pin Assignment

Figure 2: Pin Assignments for 32-lead PLCC
1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash
SST39SF010A / SST39SF020A / SST39SF040

Data Sheet

Figure 3: Pin Assignments for 32-lead TSOP (8mm x 14mm)

Figure 4: Pin Assignments for 32-pin PDIP
### Table 1: Pin Description

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Pin Name</th>
<th>Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMS1-A0</td>
<td>Address Inputs</td>
<td>To provide memory addresses. During Sector-Erase AMS-A12 address lines will select the sector.</td>
</tr>
<tr>
<td>DQ7-DQ0</td>
<td>Data Input/output</td>
<td>To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.</td>
</tr>
<tr>
<td>CE#</td>
<td>Chip Enable</td>
<td>To activate the device when CE# is low.</td>
</tr>
<tr>
<td>OE#</td>
<td>Output Enable</td>
<td>To gate the data output buffers.</td>
</tr>
<tr>
<td>WE#</td>
<td>Write Enable</td>
<td>To control the Write operations.</td>
</tr>
<tr>
<td>VDD</td>
<td>Power Supply</td>
<td>To provide 5.0V supply (4.5-5.5V)</td>
</tr>
<tr>
<td>VSS</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>NC</td>
<td>No Connection</td>
<td>Unconnected pins.</td>
</tr>
</tbody>
</table>

1. AMS = Most significant address
AMS = A16 for SST39SF010A, A17 for SST39SF020A, and A18 for SST39SF040
Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

Read

The Read operation of the SST39SF010A/020A/040 is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram (Figure 5) for further details.

Byte-Program Operation

The SST39SF010A/020A/040 are programmed on a byte-by-byte basis. Before programming, the sector where the byte exists must be fully erased. The Program operation is accomplished in three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte-Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed, within 20 µs. See Figures 6 and 7 for WE# and CE# controlled Program operation timing diagrams and Figure 16 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

Sector-Erase Operation

The Sector-Erase operation allows the system to erase the device on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 KByte. The Sector-Erase operation is initiated by executing a six-byte command load sequence for Software Data Protection with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The sector address is latched on the falling edge of the sixth WE# pulse, while the command (30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 10 for timing waveforms. Any commands written during the Sector-Erase operation will be ignored.

Chip-Erase Operation

The SST39SF010A/020A/040 provide Chip-Erase operation, which allows the user to erase the entire memory array to the “1s” state. This is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte Software Data Protection command sequence with Chip-Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the internal Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 4 for the command sequence, Figure 11 for timing diagram, and Figure 19 for the flowchart. Any commands written during the Chip-Erase operation will be ignored.
Write Operation Status Detection

The SST39SF010A/020A/040 provide two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ7) and Toggle Bit (DQ6). The End-of-Write detection mode is enabled after the rising edge of WE# which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ7 or DQ6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling (DQ7)

When the SST39SF010A/020A/040 are in the internal Program operation, any attempt to read DQ7 will produce the complement of the true data. Once the Program operation is completed, DQ7 will produce true data. Note that even though DQ7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read DQ7 will produce a ‘0’. Once the internal Erase operation is completed, DQ7 will produce a ‘1’. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector- or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 8 for Data# Polling timing diagram and Figure 17 for a flowchart.

Toggle Bit (DQ6)

During the internal Program or Erase operation, any consecutive attempts to read DQ6 will produce alternating 0s and 1s, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector- or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 9 for Toggle Bit timing diagram and Figure 17 for a flowchart.

Data Protection

The SST39SF010A/020A/040 provide both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a Write cycle.

VDD Power Up/Down Detection: The Write operation is inhibited when VDD is less than 2.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.
Software Data Protection (SDP)

The SST39SF010A/020A/040 provide the JEDEC approved Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte load sequence. The SST39SF010A/020A/040 devices are shipped with the Software Data Protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to read mode, within TRC.

Product Identification

The Product Identification mode identifies the device as the SST39SF040, SST39SF010A, or SST39SF020A and manufacturer as SST. This mode may be accessed by software operations. Users may wish to use the software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, Table 4 for software operation, Figure 12 for the software ID entry and read timing diagram and Figure 18 for the ID entry command sequence flowchart.

Table 2: Product Identification

<table>
<thead>
<tr>
<th>Manufacturer's ID</th>
<th>Address</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>SST39SF010A</td>
<td>0001H</td>
<td>B5H</td>
</tr>
<tr>
<td>SST39SF020A</td>
<td>0001H</td>
<td>B6H</td>
</tr>
<tr>
<td>SST39SF040</td>
<td>0001H</td>
<td>B7H</td>
</tr>
</tbody>
</table>

Product Identification Mode Exit/Reset

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Exit ID command sequence, which returns the device to the Read operation. Please note that the software reset command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 13 for timing waveform and Figure 18 for a flowchart.
Operations

Table 3: Operation Modes Selection

<table>
<thead>
<tr>
<th>Mode</th>
<th>CE#</th>
<th>OE#</th>
<th>WE#</th>
<th>DQ</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read</td>
<td>VIL</td>
<td>VIL</td>
<td>VIH</td>
<td>DOUT</td>
<td>AIN</td>
</tr>
<tr>
<td>Program</td>
<td>VIL</td>
<td>VIL</td>
<td>VIH</td>
<td>DIN</td>
<td>AIN</td>
</tr>
<tr>
<td>Erase</td>
<td>VIL</td>
<td>VIH</td>
<td>VIH</td>
<td>X</td>
<td>Sector address, XXH for Chip-Erase</td>
</tr>
<tr>
<td>Standby</td>
<td>VIH</td>
<td>VIH</td>
<td>VIH</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Write Inhibit</td>
<td>X</td>
<td>VIL</td>
<td>X</td>
<td>High Z/DOUT</td>
<td>X</td>
</tr>
<tr>
<td>Product Identification</td>
<td>VIL</td>
<td>VIL</td>
<td>VIH</td>
<td>See Table 4</td>
<td></td>
</tr>
</tbody>
</table>

1. X can be VIL or VIH, but no other value.

Table 4: Software Command Sequence

<table>
<thead>
<tr>
<th>Command Sequence</th>
<th>1st Bus Write Cycle</th>
<th>2nd Bus Write Cycle</th>
<th>3rd Bus Write Cycle</th>
<th>4th Bus Write Cycle</th>
<th>5th Bus Write Cycle</th>
<th>6th Bus Write Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Addr1 Data</td>
<td>Addr1 Data</td>
<td>Addr1 Data</td>
<td>Addr1 Data</td>
<td>Addr1 Data</td>
<td>Addr1 Data</td>
</tr>
<tr>
<td>Byte-Program</td>
<td>5555H AAH</td>
<td>2AAAH 55H</td>
<td>5555H A0H</td>
<td>BA2 Data</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sector-Erase</td>
<td>5555H AAH</td>
<td>2AAAH 55H</td>
<td>5555H 80H</td>
<td>5555H AAH</td>
<td>2AAAH 55H</td>
<td>5555H 30H</td>
</tr>
<tr>
<td>Chip-Erase</td>
<td>5555H AAH</td>
<td>2AAAH 55H</td>
<td>5555H 80H</td>
<td>5555H AAH</td>
<td>2AAAH 55H</td>
<td>5555H 10H</td>
</tr>
<tr>
<td>Software ID Entry4,5</td>
<td>5555H AAH</td>
<td>2AAAH 55H</td>
<td>5555H 90H</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Software ID Exit6</td>
<td>XXH F0H</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Software ID Exit6</td>
<td>5555H AAH</td>
<td>2AAAH 55H</td>
<td>5555H F0H</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. Address format A14-A0 (Hex). Addresses AMS-A15 can be VIL or VIH, but no other value, for the Command sequence.
2. AMS = Most significant address
3. AMS = AMS for SST39SF010A, A17 for SST39SF020A, and A18 for SST39SF040
4. The device does not remain in Software Product ID mode if powered down.
5. With AMS-A1 = 0; SST Manufacturer's ID = BFH, is read with A0 = 0,
   SST39SF010A Device ID = B5H, is read with A0 = 1
   SST39SF020A Device ID = B6H, is read with A0 = 1
   SST39SF040 Device ID = B7H, is read with A0 = 1
6. Both Software ID Exit operations are equivalent
**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias .................................................. -55°C to +125°C  
Storage Temperature ......................................................... -65°C to +150°C  
D. C. Voltage on Any Pin to Ground Potential ...................... -0.5V to VDD+0.5V  
Transient Voltage (<20 ns) on Any Pin to Ground Potential ...... -2.0V to VDD+2.0V  
Voltage on A9 Pin to Ground Potential ............................... -0.5V to 13.2V  
Package Power Dissipation Capability (Ta = 25°C) ................... 1.0W  
Through Hold Lead Soldering Temperature (10 Seconds) .......... 300°C  
Surface Mount Lead Soldering Temperature (3 Seconds) .......... 240°C  
Output Short Circuit Current1 .......................................... 100 mA  

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

**Table 5: Operating Range**

<table>
<thead>
<tr>
<th>Range</th>
<th>Ambient Temp</th>
<th>V&lt;sub&gt;DD&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial</td>
<td>0°C to +70°C</td>
<td>4.5-5.5V</td>
</tr>
<tr>
<td>Industrial</td>
<td>-40°C to +85°C</td>
<td>4.5-5.5V</td>
</tr>
</tbody>
</table>

**Table 6: AC Conditions of Test<sup>1</sup>**

<table>
<thead>
<tr>
<th>Input Rise/Fall Time</th>
<th>Output Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>5ns</td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 30 pF for 55 ns</td>
</tr>
<tr>
<td></td>
<td>C&lt;sub&gt;L&lt;/sub&gt; = 100 pF for 70 ns</td>
</tr>
</tbody>
</table>

1. See Figures 14 and 15
Table 7: DC Operating Characteristics $V_{DD} = 4.5-5.5V$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{DD}$</td>
<td>Power Supply Current</td>
<td></td>
<td>Address input=$V_{IL}/V_{IH}$, at $f=1/T_{RC}$ Min $V_{DD}=V_{DD}$ Max</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>25 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Max</td>
<td>35 mA</td>
</tr>
<tr>
<td>$I_{SB1}$</td>
<td>Standby $V_{DD}$ Current (TTL input)</td>
<td>3 mA</td>
<td>$CE#=V_{IH}, V_{DD}=V_{DD}$ Max</td>
</tr>
<tr>
<td>$I_{SB2}$</td>
<td>Standby $V_{DD}$ Current (CMOS input)</td>
<td>100 $\mu A$</td>
<td>$CE#=V_{IH}, V_{DD}=V_{DD}$ Max</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Leakage Current</td>
<td>1 $\mu A$</td>
<td>$V_{IN}=GND$ to $V_{DD}, V_{DD}=V_{DD}$ Max</td>
</tr>
<tr>
<td>$I_{OL}$</td>
<td>Output Leakage Current</td>
<td>10 $\mu A$</td>
<td>$V_{OUT}=GND$ to $V_{DD}, V_{DD}=V_{DD}$ Max</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td>0.8 V</td>
<td>$V_{DD}=V_{DD}$ Min</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>2.0 V</td>
<td>$V_{DD}=V_{DD}$ Max</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage (CMOS input)</td>
<td>0.3 V</td>
<td>$V_{DD}=V_{DD}$ Max</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage</td>
<td>0.4 V</td>
<td>$I_{OL}=2.1 mA, V_{DD}=V_{DD}$ Min</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage</td>
<td>2.4 V</td>
<td>$I_{OH}=400 \mu A, V_{DD}=V_{DD}$ Min</td>
</tr>
</tbody>
</table>

1. Typical conditions for the Active Current shown on the front data sheet page are average values at 25°C (room temperature), and $V_{DD} = 5V$ for SF devices. Not 100% tested.
2. Values are for 70 ns conditions. See the Multi-Purpose Flash Power Rating application note for further information.

Table 8: Recommended System Power-up Timings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{PU-READ}$</td>
<td>Power-up to Read Operation</td>
<td>100 µs</td>
<td>µs</td>
</tr>
<tr>
<td>$T_{PU-WRITE}$</td>
<td>Power-up to Program/Erase Operation</td>
<td>100 µs</td>
<td>µs</td>
</tr>
</tbody>
</table>

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 9: Capacitance ($Ta = 25°C, f=1$ Mhz, other pins open)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Condition</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{VO}$</td>
<td>I/O Pin Capacitance</td>
<td>$V_{IO} = 0V$</td>
<td>12 pF</td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Input Capacitance</td>
<td>$V_{IN} = 0V$</td>
<td>6 pF</td>
</tr>
</tbody>
</table>

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 10: Reliability Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum Specification</th>
<th>Units</th>
<th>Test Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N_{END}$</td>
<td>Endurance</td>
<td>10,000 Cycles</td>
<td></td>
<td>JEDEC Standard A117</td>
</tr>
<tr>
<td>$T_{DR}$</td>
<td>Data Retention</td>
<td>100 Years</td>
<td></td>
<td>JEDEC Standard A103</td>
</tr>
<tr>
<td>$I_{LTH}$</td>
<td>Latch Up</td>
<td>100 + $I_{DD}$</td>
<td></td>
<td>JEDEC Standard 78</td>
</tr>
</tbody>
</table>

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. $N_{END}$ endurance rating is qualified as a 10,000 cycle minimum for the whole device. A sector- or block-level rating would result in a higher minimum specification.
### AC Characteristics

#### Table 11: Read Cycle Timing Parameters $V_{DD} = 4.5$-$5.5$V

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>SST39SF010A/020A/040-55</th>
<th>SST39SF010A/020A/040-70</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>TRC</td>
<td>Read Cycle Time</td>
<td>55</td>
<td>70</td>
</tr>
<tr>
<td>TCE</td>
<td>Chip Enable Access Time</td>
<td>55</td>
<td>70</td>
</tr>
<tr>
<td>TAA</td>
<td>Address Access Time</td>
<td>55</td>
<td>70</td>
</tr>
<tr>
<td>TDE</td>
<td>Output Enable Access Time</td>
<td>35</td>
<td>35</td>
</tr>
<tr>
<td>TCLZ$^1$</td>
<td>CE# Low to Active Output</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>TOLZ$^1$</td>
<td>OE# Low to Active Output</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>TCHZ$^1$</td>
<td>CE# High to High-Z Output</td>
<td>20</td>
<td>25</td>
</tr>
<tr>
<td>TOHZ$^1$</td>
<td>OE# High to High-Z Output</td>
<td>20</td>
<td>25</td>
</tr>
<tr>
<td>TOH$^1$</td>
<td>Output Hold from Address Change</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

#### Table 12: Program/Erase Cycle Timing Parameters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>TBP</td>
<td>Byte-Program Time</td>
<td>20</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>TAS</td>
<td>Address Setup Time</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TAH</td>
<td>Address Hold Time</td>
<td>30</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TCS</td>
<td>WE# and CE# Setup Time</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TCH</td>
<td>WE# and CE# Hold Time</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TOES</td>
<td>OE# High Setup Time</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TOEH</td>
<td>OE# High Hold Time</td>
<td>10</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TCP</td>
<td>CE# Pulse Width</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TWP</td>
<td>WE# Pulse Width</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TWP$^1$</td>
<td>WE# Pulse Width High</td>
<td>30</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TCP$^1$</td>
<td>CE# Pulse Width High</td>
<td>30</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TDS</td>
<td>Data Setup Time</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TDH$^1$</td>
<td>Data Hold Time</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TDA$^1$</td>
<td>Software ID Access and Exit Time</td>
<td>150</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TSE</td>
<td>Sector-Erase</td>
<td>25</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>TSC$^1$</td>
<td>Chip-Erase</td>
<td>100</td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
1 Mbit / 2 Mbit / 4 Mbit Multi-Purpose Flash
SST39SF010A / SST39SF020A / SST39SF040

Data Sheet

Figure 5: Read Cycle Timing Diagram

Figure 6: WE# Controlled Program Cycle Timing Diagram

Note: AMS = Most significant address
AMS = A16 for SST39SF010A, A17 for SST39SF020A, and A18 for SST39SF040
Figure 7: CE# Controlled Program Cycle Timing Diagram

Figure 8: Data# Polling Timing Diagram

Note: 
AMS = Most significant address
AMS = A16 for SST39SF010A, A17 for SST39SF020A, and A18 for SST39SF040
Figure 9: Toggle Bit Timing Diagram

Note: Toggled bit output is always high first.
AMS = Most significant address
AMS = A16 for SST39SF010A, A17 for SST39SF020A, and A18 for SST39SF040

Figure 10: WE# Controlled Sector-Erase Timing Diagram

Note: This device also supports CE# controlled Sector-Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 10)
SAx = Sector Address
Toggled bit output is always high first.
AMS = Most significant address
AMS = A16 for SST39SF010A, A17 for SST39SF020A, and A18 for SST39SF040
Figure 11: WE# Controlled Chip-Erase Timing Diagram

Note: This device also supports CE# controlled Sector-Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 10)
SA<xx> = Sector Address
Toggled bit output is always high first.
AMS = Most significant address

Figure 12: Software ID Entry and Read

Note: Device ID = B5H for SST39SF010A, B6H for SST39SF020A, and B7H for SST39SF040
Figure 13: Software ID Exit and Reset

Figure 14: AC Input/Output Reference Waveforms

AC test inputs are driven at $V_{IH}$ (3.0V) for a logic “1” and $V_{IL}$ (0V) for a logic “0”. Measurement reference points for inputs and outputs are $V_{IT}$ (1.5V) and $V_{OT}$ (1.5V). Input rise and fall times (10% $\rightarrow$ 90%) are <5 ns.

Note: $V_{IT}$ - $V_{INPUT}$ Test  
$V_{OT}$ - $V_{OUTPUT}$ Test  
$V_{IH}$ - $V_{INPUT}$ HIGH Test  
$V_{IL}$ - $V_{INPUT}$ LOW Test

Figure 15: A Test Load Example
Figure 16: Byte-Program Algorithm
Figure 17: Wait Options

- **Internal Timer**
  - Byte Program/Erase Initiated
  - Wait TBP, TSCE, or TSE
  - Program/Erase Completed

- **Toggle Bit**
  - Byte Program/Erase Initiated
  - Read byte
  - Read same byte
  - Does DQ6 match?
    - No
    - Yes
      - Program/Erase Completed

- **Data# Polling**
  - Byte Program/Erase Initiated
  - Read DQ7
  - Is DQ7 = true data?
    - No
    - Yes
      - Program/Erase Completed
**Software Product ID Entry Command Sequence**

- Load data: AAH  
  Address: 5555H

- Load data: 55H  
  Address: 2AAAAH

- Load data: 90H  
  Address: 5555H

- Wait T\text{IDA}

- Read Software ID

---

**Software Product ID Exit & Reset Command Sequence**

- Load data: AAH  
  Address: 5555H

- Load data: 55H  
  Address: 2AAAAH

- Load data: F0H  
  Address: 5555H

- Wait T\text{IDA}

- Return to normal operation

---

**Figure 18:** Software Product Command Flowcharts
**Figure 19:** Erase Command Sequence

**Chip-Erase Command Sequence**

1. Load data: AAH  
   Address: 5555H
2. Load data: 55H  
   Address: 2AAAH
3. Load data: 80H  
   Address: 5555H
4. Load data: AAH  
   Address: 5555H
5. Load data: 55H  
   Address: 2AAAH
6. Load data: 10H  
   Address: 5555H
7. Wait TSCE
8. Chip erased to FFH

**Sector-Erase Command Sequence**

1. Load data: AAH  
   Address: 5555H
2. Load data: 55H  
   Address: 2AAAH
3. Load data: 80H  
   Address: 5555H
4. Load data: 55H  
   Address: 2AAAH
5. Load data: 30H  
   Address: SAX
6. Load data: AAH  
   Address: 5555H
7. Wait TSE
8. Sector erased to FFH
## Product Ordering Information

<table>
<thead>
<tr>
<th>SST</th>
<th>39</th>
<th>SF</th>
<th>010A</th>
<th>-</th>
<th>70</th>
<th>-</th>
<th>4C</th>
<th>-</th>
<th>NHE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>XX</td>
<td>XX</td>
<td>XXXX</td>
<td>-</td>
<td>XX</td>
<td>-</td>
<td>XX</td>
<td>-</td>
<td>XXX</td>
</tr>
</tbody>
</table>

### Environmental Attribute

- \( E^1 \) = non-Pb

### Package Modifier

- \( H \) = 32 pins or leads

### Package Type

- \( N \) = PLCC
- \( P \) = PDIP
- \( W \) = TSOP (type 1, die up, 8mm x 14mm)

### Temperature Range

- \( C \) = Commercial = 0°C to +70°C
- \( I \) = Industrial = -40°C to +85°C

### Minimum Endurance

- 4 = 10,000 cycles

### Read Access Speed

- 55 = 55 ns
- 70 = 70 ns

### Version

- A = Special Feature Version

### Device Density

- 040 = 4 Mbit
- 020 = 2 Mbit
- 010 = 1 Mbit

### Voltage

- S = 4.5-5.5V

### Product Series

- 39 = Multi-Purpose Flash

---

1. Environmental suffix “E” denotes non-Pb solder. SST non-Pb solder devices are “RoHS Compliant.”
Valid combinations for SST39SF010A

<table>
<thead>
<tr>
<th>Combination 1</th>
<th>Combination 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>SST39SF010A-55-4C-NHE</td>
<td>SST39SF010A-55-4C-WHE</td>
</tr>
<tr>
<td>SST39SF010A-70-4C-NHE</td>
<td>SST39SF010A-70-4C-WHE</td>
</tr>
<tr>
<td>SST39SF010A-55-4I-NHE</td>
<td>SST39SF010A-55-4I-WHE</td>
</tr>
<tr>
<td>SST39SF010A-70-4I-NHE</td>
<td>SST39SF010A-70-4I-WHE</td>
</tr>
</tbody>
</table>

Valid combinations for SST39SF020A

<table>
<thead>
<tr>
<th>Combination 1</th>
<th>Combination 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>SST39SF020A-55-4C-NHE</td>
<td>SST39SF020A-55-4C-WHE</td>
</tr>
<tr>
<td>SST39SF020A-70-4C-NHE</td>
<td>SST39SF020A-70-4C-WHE</td>
</tr>
</tbody>
</table>

Valid combinations for SST39SF040

<table>
<thead>
<tr>
<th>Combination 1</th>
<th>Combination 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>SST39SF040-55-4C-NHE</td>
<td>SST39SF040-55-4C-WHE</td>
</tr>
<tr>
<td>SST39SF040-70-4C-NHE</td>
<td>SST39SF040-70-4C-WHE</td>
</tr>
<tr>
<td>SST39SF040-55-4I-NHE</td>
<td>SST39SF040-55-4I-WHE</td>
</tr>
<tr>
<td>SST39SF040-70-4I-NHE</td>
<td>SST39SF040-70-4I-WHE</td>
</tr>
</tbody>
</table>

**Note:** Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.
Packaging Diagrams

**Figure 20:** 32-lead Plastic Lead Chip Carrier (PLCC)
SST Package Code: NH

Note: 1. Complies with JEDEC publication 95 MS-016 AE dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (max/min).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
Figure 21: 32-lead Thin Small Outline Package (TSOP) 8mm x 14mm
SST Package Code: WH

Note: 1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25 mm between leads.
Figure 22: 32-pin Plastic Dual In-line Pins (PDIP)

SST Package Code: PH

Note:
1. Complies with JEDEC publication 95 MO-015 AP dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (max/min).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .010 inches.
Table 13: Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Description</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>02</td>
<td>2002 Data Book</td>
<td>May 2002</td>
</tr>
</tbody>
</table>
| 03       | Changes to Table 7 on page 12  
Added footnote for MPF power usage and Typical conditions  
Clarified the Test Conditions for Power Supply Current and Read parameters  
Clarified $I_{DD}$ Write to be Program and Erase | Mar 2003   |
| 04       | Document status changed from “Preliminary Specification” to “Data Sheet”  
Changed $I_{DD}$ Program and Erase max values from 25 to 35 in Table 7 on page 12 | Oct 2003   |
| 05       | 2004 Data Book  
Added non-Pb MPNs and removed footnote (See page 24) | Nov 2003   |
| 06       | Corrected Revision History for Version 04:  
$I_{DD}$ max value was incorrectly stated as 30 mA instead of 35 mA | Aug 2004   |
| 07       | Removed leaded parts from valid combinations. See PSN-D0PB0001 | Mar 2009   |
| 08       | Changed endurance from 10,000 to 100,000 in Product Description, page 1 | Sep 2009   |
| 09       | End of Life for all 45 ns valid combinations. See S71147(02).  
Added replacement 55 ns valid combinations | Jan 2010   |
| A        | All 45 ns parts reinstated.  
Applied new document format  
Released document under letter revision system  
Updated spec number from S71147 to DS25022 | Jul 2011   |
| B        | End of Life for all 45 ns valid combinations.  
Updated Table 6 and Table 11 | Apr 2013   |


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SST makes no warranty for the use of its products other than those expressly contained in the Standard Terms and Conditions of Sale.

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