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SiC Schottky Diodes for Harsh Environment Space Applications

Philippe Godignon, Xavier Jordà, Miquel Vellvehi, Xavier Perpiñà, Viorel Banu, Demetrio López, Juan Barbero, Pierre Brosselard, and Silvia Massetti

Abstract—This paper reports on the fabrication technology and packaging strategy for 300-V 5-A silicon carbide Schottky diodes with a wide temperature operation range capability (between $-170 \, ^\circ\text{C}$ and $300 \, ^\circ\text{C}$). These diodes have been designed for harsh environment space applications such as inner Solar System exploration probes. Different endurance tests have been performed to evaluate the diode behavior when working at a high temperature and under severe thermal cycling conditions (ranged from $-170 \, ^\circ\text{C}$ to $270 \, ^\circ\text{C}$). The radiation hardness capability has been also tested. It has been found that the hermeticity of the package in a neutral atmosphere is a key aspect to avoid an electrical parameter drift. Moreover, the use of gold metallization and gold wire bonds on the anode allows reducing the diode surface and bonding degradation when compared to Al-containing technology. On the back-side cathode contact, the Ti/Ni/Au metallization and AuGe combination have shown a very good behavior. As a result, the manufactured diodes demonstrated high stability for a continuous operation at $285 \, ^\circ\text{C}$.

Index Terms—High temperature, packaging, radiation hardness, Schottky diodes, silicon carbide (SiC), space electronics.

I. INTRODUCTION

The increasing demand for high-temperature electronics has stimulated the research for alternatives to silicon (Si) which are capable to operate under extreme working conditions, e.g., in harsh environment, at temperature above $300 \, ^\circ\text{C}$, under high pressures, experiencing intense vibrations, or withstanding corrosive liquids. Wide-bandgap semiconductors are materials that have attracted much attention, particularly due to their superior electrical, mechanical, and chemical properties. Currently, the wide-bandgap material which presents a more mature manufacturing technology is SiC. The recent improvements in SiC material growth, with a strong reduction of the defect density in the starting material, have allowed producing reliable SiC-based devices [1], [2]. This fact has conferred SiC to be the most adequate candidate for developing high-efficiency converters and high-power electronics [3]–[5]. The most advanced device from the technical and commercial points of view is the Schottky diode [6], [7]. Commercial diodes produced by Infineon or Cree, Inc., have shown to be efficient and reliable in standard power applications [8]. Schottky SiC-based devices are an interesting solution for the ever increasing demand required by space applications, such as BepiColombo mission [9].

The BepiColombo mission will consist of two separate spacecraft that will orbit Mercury. Since Mercury is close to the Sun, the expected working temperature of the solar cell and related electronics ranges from $-170 \, ^\circ\text{C}$ to $+270 \, ^\circ\text{C}$. In particular, the Mercury Planetary Orbiter (MPO) will be exposed to Sun intensities up to 10.7 times higher than in the Earth’s orbit. The high operating temperature is not the only challenge of this mission. When orbiting around Mercury, the MPO will experience seasonal eclipses. The minimum expected temperature in an eclipse is $-170 \, ^\circ\text{C}$, and the number of cycles is in the range of 4000. Therefore, this application requires that operating conditions of the blocking diodes must be extended far beyond the limits of existing high-reliability diodes.

This paper, conducted under a Thales Alenia Space, Turin, contract, aims to develop Schottky SiC-based devices capable to be used in the BepiColombo mission. However, the package of the commercially available devices is designed for a maximum junction temperature of 175 $^\circ\text{C}$. Regarding our BepiColombo application, 300-V 5-A diodes are required with a working temperature capability ranging from $-170 \, ^\circ\text{C}$ to $270 \, ^\circ\text{C}$. The two main challenges to extend the diodes’ state of the art to this particular temperature range were as follows: to define a reliable high-temperature package and to modify accordingly the SiC die technology to fit in the novel package. Different technological approaches have been considered, with main variations on the interconnection technique and metallization layers. Batches of packaged diodes have been submitted to long-term electrical stress to define the optimal design and process flow chart for the diode, focusing on the device stability in dc mode. Thermal cycling tests have also been performed to evaluate the thermomechanical stability.

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**II. SEMICONDUCTOR DEVICE PROCESSING**

The SiC Schottky diodes have been processed on 4H-SiC wafers supplied by CREE Research, Inc. The epilayer is 5 μm thick and doped in $1 \times 10^{16}$ cm$^{-3}$. The high-voltage edge termination is made with the so-called junction termination extension (JTE) technique. The JTE is implemented through aluminum implantation done at a high temperature (300 °C), followed by an annealing step at 1600 °C for 30 min. SiO$_2$ was used as the surface passivation layer. These processing steps are similar to the ones used for standard temperature range diodes [10]. The high-temperature capability of the semiconductor die is mainly given by the selection of the metallization schemes. However, the choice of these metallization schemes is strongly linked to the packaging technology. A typical Schottky diode is made of a first thin metal layer (Metal 1) to form the Schottky contact on the semiconductor surface. On the top of this contact metallization, we add a thick layer (few micrometers) of metal (Metal 2) in order to reduce the parasitic resistance of the thin contact metal (Metal1) and to increase the diode current capability. We already reported in [11] that the titanium (Ti) and nickel (Ni) metal layers typically used commercially and our standard SiC Schottky diodes were not suitable for a high-temperature operation. Forward voltage drift and double barrier effects with Ni and high reverse leakage currents with Ti are observed in these diodes under a high-temperature operation. This is why we used tungsten (W) metallization as the Schottky contact in our high-temperature diodes. Regarding the thick metallization (Metal 2), aluminum (Al) is typically used in standard power electronic rectifiers. However, we have evidenced that a thick gold (Au) layer is more suitable regarding the packaging technology we choose, as it will be shown later in this paper. The back-side ohmic contact is made with Ni. This contact has been proved to be stable for temperatures below 300 °C. For the final back-side metallization, we kept our standard Ti/Ni/Au metallization scheme. Finally, we did not use the thick polyimide passivation usually present in standard diodes to avoid any out-gazing effects. This approach can be done for diodes with breakdown voltages up to 1.6 kV. For higher breakdown voltages, an innovative solution should be found to make the high-voltage and high-temperature capabilities compatible.

**III. PACKAGING STRATEGY**

The packaging of high-temperature SiC-based components is a challenging task, mainly requiring the compatibility of electrical, thermal, and mechanical properties of the involved materials [12]. The packaging specifications of the proposed component have been fulfilled, taking, as a departure point, a modified TO-257 metallic package from Kyocera. Fig. 1 shows a cross-sectional scheme of the package and its main parts. On the bottom, a 1-mm-thick WCu flange ensures appropriate thermal contact with the corresponding heat-extraction system, provides a mounting hole, and provides also the required thermomechanical stability to ensure long-term reliability under temperature cycling. Over this gold-plated flange, a BeO slab is bonded with Ag. This 635-μm-thick ceramic layer ensures electric isolation between the die and the case, as well as an adequate heat extraction capability. Thermal properties of ceramics are difficult to evaluate because they depend on the fabrication process, impurity contents, etc., but typical values for the BeO thermal conductivity are 285 W/m · K at 25 °C and less than 100 W/m · K at 300 °C [13]. On the top of the BeO, a metallization of 50-μm Ni plus 50-μm Au is provided for chip attachment. The lateral frame of the case is made with gold-plated Cu, and it shows three ceramic through-holes for pin access. The combination of Cu alloy pins plus ceramic through-hole is optimized to guarantee hermeticity in a wide temperature range. One of the pins (the cathode one) is directly connected to the Ni/Au metallization over the BeO slab while the two remaining pin tips are suitable for wire bonding toward the anode pad. Finally, the TO-257 case is completed with a Ni cap placed on the top using a seam sealing process in order to close hermetically the housing, under a neutral ambient of pure N$_2$.

Two critical points of the assembly process concern the die front- and back-side interconnections. The back-side interconnection must provide correct thermal and electrical contacts, as well as good mechanical stability in the whole operation range. The selected die-attach material was the eutectic Au88/Ge12 alloy, showing acceptable thermal (44 W/m · K) and electrical (15 μΩm) conductivities, as well as a moderate coefficient of thermal expansion (13.4 ppm/K). Its melting point (358 °C) allows operation temperatures around 300 °C and is compatible with relatively standard soft-soldering techniques. In this sense, the die-attach process was performed on a static reflow oven where the chip was placed over a 50-μm-thick AuGe squar preform. The process was optimized by adjusting the temperature profile slopes (heating and cooling phases), the ambient (reductive in a first phase and vacuum in a second phase), the peak temperature (value and time), and the pressure applied to the die.

Fig. 2 shows the scanning acoustic microscope (C-SAM) images taken to evaluate the die-attach soldering process with a Sonoscan Gen-5 acoustic microscope. Fig. 2(a) shows the square die-attach layer in gray while the voids appear in white. As it can be appreciated, the void content is very low (below 3% area), and the dark ellipse in the lower right corner corresponds to the mentioned contact between the BeO metallization and the cathode pin. As the 100-MHz ultrasound wave reaches the AuGe layer through the flange, Ag, and BeO stack, the defects in these layers could appear as shadows on the AuGe C-SAM image. Thus, the image of Fig. 2(b) is focused on the Ag layer between the flange and the BeO and shows, in white, the voids.
of the Ag. As it can be observed, there are a few voids in the Ag around its central area (where the die is placed), but they are small. The die-shear tests performed on six diodes after the life tests described in the next sections have shown minimum values of 6 kgf (10.5 MPa) for the proposed die-attach layer which is well above the minimum required value, and three of the samples show a shear force of above 10 kgf. In addition, a severe thermal cycling test campaign has also been started. The elementary cycle begins with the devices at $-170^\circ C$ for 15 min. Then, the temperature rises up to $+270^\circ C$ in less than 20 min, remains at this value for 15 min, and descends again to $-170^\circ C$ (maximum slopes of 40 $^\circ C$/min). After 4000 cycles under the described conditions, any significant drift of the electrical characteristics has been observed, and neither diode has failed. Therefore, the proposed Ti/Ni/Au back-side metallization and AuGe die-attach combination seem to be very stable, allowing higher temperature operations than previously reported for SiC devices using this alloy [14]. Die-shear tests of the cycled diodes will be performed to confirm the integrity of the cathode contact, although the results are not available at this moment.

The front-side anode contact is also a critical part of the assembly. Due to the severe temperature conditions, the connection between the 3-μm-thick Au anode pad and the anode pins of the package is performed with 50-μm Au wire bonds. There are ten parallel wires in total, soldered by ultrasonic ball bonding and distributed to the two anode pins. The bond-pull tests performed on diode samples have shown mean rupture forces of 18 gf and good adhesion at both wire edges: at the ball bonding in the diode side and at the stitch bonding in the pin side.

IV. THERMAL RESISTANCE CHARACTERIZATION

At high operation temperatures, the component capability for heat dissipation becomes a very critical issue. If the thermal resistance value between the device junction and the case is not low enough, the chip could easily exceed its maximum allowed temperature when the component is in a high-temperature ambient. In addition, practically all materials involved in the packaging assembly process show a thermal conductivity reduction with temperature. Thus, the characterization of the junction-to-case thermal resistance ($R_{TH(j-c)}$) in the critical operation range is of main importance. $R_{TH(j-c)}$ determination has been tackled by direct junction temperature measurement using an IR camera in open components (without the Ni cap) and by junction temperature estimation through a temperature-sensitive parameter in closed packages [15]. Both approaches have shown the same results. The die area is 5.7 mm$^2$, and the die thickness is 360 μm. The device under test is placed over a temperature-controlled plate acting as a heat sink. This allows the temperature measurement of the package flange surface with a spring-loaded K-type thermocouple located below the die. This temperature is considered the reference case temperature. To determine $R_{TH(j-c)}$, the required heating current is applied in order to obtain a given dissipated power. The junction ($T_j$) and case ($T_C$) temperatures are recorded, allowing the plot of the temperature increment ($T_j - T_C$)-versus-dissipated-power curves. Fig. 3(a) shows one of such plots for a measurement process at room temperature. It is interesting to observe that, even with a suitable thermal interface material between the case and the heat sink, the case temperature experiences a significant temperature variation, and it must be monitored during the tests. The $R_{TH(j-c)}$ value at each temperature is evaluated as the slope of the temperature-increment-versus-power plot when the baseplate is controlled at the prefixed
Fig. 4. Evolution of the $R_{TH(j\rightarrow c)}$ between 25 °C and 300 °C.

Fig. 5. Forward $I$–$V$ characteristics of one diode measured at three different temperatures.

V. STABILITY AND LIFE TESTS

Diodes have been first measured in forward and reverse modes at $-170$ °C, room temperature, and 270 °C. The $I$–$V$ curve in the forward mode is shown in Fig. 5, and reverse current values at 300 V of one representative diode at different temperatures are listed in Table I.

To assess the potential degradation of the forward and reverse characteristics for the high-temperature environment, endurance tests have been performed. These tests consist in forward biasing the diodes for more than 500 h at different ambient temperatures higher than 285 °C. The test is performed in an inert atmosphere ($N_2$) chamber, and the diodes are dc biased at 5 A. Each endurance test was performed on ten samples connected in series on a common aluminum heat sink. The reference temperature is taken on the heat sink while the temperature of each diode is also recorded (thermocouple fixed on the top of each diode case). The chamber temperature was regulated to get the test temperature when the diodes were biased at 5 A in order to take into account the increase of temperature due to the self-heating. We also performed temperature stress steps consisting in having the parts at a starting temperature of 230 °C during 96 h. The next step consisted in increasing the temperature by 10 °C and stressing the diodes for 96 h successively [16]. Finally, we also performed a combination of the endurance test with high-temperature reverse bias stress (HTRB). Table II summarizes the different stress tests applied to the diodes.

Fig. 6 shows the evolution of the forward and reverse characteristics of a Schottky diode after 2000 h of stress at 285 °C. As we can appreciate, there is no drift of the forward characteristics. In the reverse mode, we observed an initial decrease of the leakage current at 300 V after the first 100 h of stress. Then, the reverse current remains stable. It indicates that a preconditioning stress is necessary before using the diodes in order to stabilize the reverse characteristics. If we measure the low-current characteristics of the diodes before and after stressing them, we do not observe any significant differences, as can be seen in the example of Fig. 7. The ideality factor and barrier height extracted before and after the endurance stress or temperature step stress are similar. Then, the decrease of the leakage current is not due to an overall variation of the barrier. However, it is possible that very local variation and improvement of the barrier height in defective areas of the

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TABLE I

<table>
<thead>
<tr>
<th>Current Value</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_p$ at 300V</td>
<td>$-170$ °C</td>
</tr>
<tr>
<td>$I_p$ at 300V</td>
<td>$+25$ °C</td>
</tr>
<tr>
<td>$I_p$ at 300V</td>
<td>$+270$ °C</td>
</tr>
</tbody>
</table>

TABLE II

<table>
<thead>
<tr>
<th>Test Type</th>
<th>Diode bias</th>
<th>Temperature</th>
<th>Hours</th>
<th>Parts failed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Endurance test 1</td>
<td>DC bias 5A</td>
<td>$285$ °C</td>
<td>2000</td>
<td>0</td>
</tr>
<tr>
<td>Endurance test 2</td>
<td>DC bias 5A</td>
<td>$300$ °C</td>
<td>1000</td>
<td>0</td>
</tr>
<tr>
<td>Endurance test 3</td>
<td>DC bias 5A</td>
<td>$330$ °C</td>
<td>500</td>
<td>1</td>
</tr>
<tr>
<td>Temperature step test</td>
<td>0V</td>
<td>From $230$ till $370$ °C</td>
<td>96 hours every T° step</td>
<td>0</td>
</tr>
<tr>
<td>HTRB</td>
<td>$-300$V</td>
<td>$270$ °C</td>
<td>500</td>
<td>0</td>
</tr>
</tbody>
</table>
Schottky contact can lead to a reduction of the leakage currents. In this way, the macroscopic barrier value of the contact does not change, but local leakage current paths due to low barrier patches caused by local defects [17] are progressively removed with the thermal stress. Another possible reason for the leakage current reduction could be due to an improvement or stabilization of the charge effects in the device periphery.

Fig. 6.  (a) Forward characteristics after different duration of endurance stress.  (b) Reverse characteristics after different duration of endurance stress.

Fig. 7.  Forward $I$–$V$ characteristics at low current of a diode before and after endurance stress at 300 $^\circ$C during 1000 h.

We have performed similar endurance tests at 300 $^\circ$C (1000 h) and 330 $^\circ$C (500 h). After 1000 h at 300 $^\circ$C, we had no drift of the forward characteristics and a similar behavior than the previously observed one in the reverse mode, as shown in Fig. 7. It is only when we stressed the devices at 330 $^\circ$C that we observed the first failure (one diode over ten). In this diode, the forward voltage drifted 10% after 500 h of stress. The reverse mode was stable. The package of this diode was analyzed using the C-SAM and bond-pull techniques. From the C-SAM images before and after the stress, we cannot observe a clear degradation of the back-side solder. Neither delamination nor increase of void density and size is seen (see Fig. 8). The variations observed between the C-SAM images of the die attach on Fig. 2(a) are mainly due to the small scratches that appeared on the flange surface after the assembly and disassembly processes using a hard thermal interface material.

The bond-pull test has been performed on all the wires of the failing diode. From the ten gold wires, nine exhibited a bond strength higher than 20 gf. Only one wire failed with a bond strength of 3.9 gf. All the wires except one remain attached to the die and to the pin after the bond pull. The only wire which failed ripped off the thick metallization of the diode.

However, it is not clear whether this failure is due to the operation temperature or to a local metallization weakness created during the fabrication process.

The temperature step stress was performed up to a diode case temperature of 370 $^\circ$C. At this temperature, we do not observe degradation of the diodes neither in the forward (see Fig. 9) nor reverse mode. This results clearly state that the back-side soldering is able to withstand higher temperatures than the Au88/Ge12 alloy melting point (358 $^\circ$C). This is due to the fact that the melting point of the AuGe alloy increases with the Au content. When we soldered the AuGe preform on the top of the Au-plated BeO slab, part of this Au diffuses, and we increased the Au percentage in the alloy, increasing in this way the maximum working temperature allowed by the AuGe alloy.

The HTRB has been also performed. Indeed, we combined 1000 h of 5-A dc stress at 230 $^\circ$C, followed by 500 h in reverse bias ($-300$ V) at 270 $^\circ$C and followed by 500 extra h of dc stress at 5-A 230 $^\circ$C. As it can be seen in Fig. 10, after the initial reverse leakage current decrease already commented, there is no drift of the reverse current after the different steps of the forward dc bias and HTRB.
We want to stress that the hermetic sealing in a neutral atmosphere is absolutely compulsory to get a stable operation of these devices at a high temperature. To confirm this, we performed the endurance test 1 (5 A and 285 °C) on devices which were not hermetically sealed. The case was welded but with a given content of oxygen inside the package (5%–18%). As we can infer from Fig. 11, we observe a progressive drift of the forward characteristics of the diodes with the endurance stress time.

This is linked to the presence of oxygen inside the package, which affects both the top metallization layers and the backside layers. We clearly observed a different aspect and color of the top metallization after the stress when compared to the initial devices. However, it is worth to note that the bond strength of the wire bonding is higher than 20 gf on these samples, indicating that the bonding is not affected by the oxygen degradation. We also observed that, if we increase the stress temperature to 330 °C, the die can be detached off the case by die shear with a force lower than 1 kgf. The oxygen seems to affect the parasitic resistance of the top metal layers. The extracted values of the Schottky barrier and the ideality factor of the Schottky contact are very similar before and after the forward voltage drift, indicating that the degradation is only affecting the resistive components of the diode. The oxygen cannot modify the SiC layer properties since the diffusion coefficient of oxygen in SiC is extremely low. The impact of the oxygen is then mainly on the metal layers and interfaces of the metal stacks. On the other hand, for this application, organic protection layers such as glob top are not recommended to avoid outgassing.

### VI. Radiation Tests

Since the proposed devices are designed for a space application in the inner Solar System, radiation tests have been performed on the diodes. Gamma rays have been first applied to the diodes, with a dose up to 570 krd and a rate of 3.6 krd/h. Table III summarizes the forward and reverse electrical parameters before and just after irradiation on five parts. As we can infer, no significant change in the forward characteristics is seen. In the reverse mode, we observe an increase of the reverse leakage current. Even if we remain with very low leakage current levels, the current increase after the stress is significant. However, if we measure again the reverse current of the diodes several days after the irradiation, the measured values are similar to the initial one. The effect of gamma irradiation on the diode behavior is then reversible. This type of behavior is a characteristic of a semiconductor interface with charges [18]. The silicon carbide interface usually presents at least one order of magnitude of interface charges higher than silicon [19].
Fast and slow traps are filled with charge during the irradiation. After a given time, depending on the trap capture cross section and the time constants, the traps return to their initial state. This directly affects the leakage current of the diode.

Proton irradiation has been evaluated on these devices. The test has been done according to the following conditions: Three samples (D30, D33, and D41) have been submitted to an energy of 100 MeV until a fluence of $10^{11}$ particles/cm$^2$. Other three samples (D65, D66, and D99) have been submitted to an energy of 60 MeV and the same fluence. Finally, three more samples (D100, D102, and D106) have been submitted to an energy of 15 MeV. These values have been defined by the customer regarding its application. Each sample was reverse biased at 200 V during the test. Resistors in series have been used to limit the current to 1 mA. The overall current of the nine samples has been monitored during the test. The irradiation was performed at room temperature. The results are listed in Table IV.

In the forward mode, we do not detect any significant impact of the proton irradiation up to the tested fluence of $1.6 \times 10^{11}$ particles/cm$^2$ for the energies of 60 and 100 MeV. For the lowest energy, 15 MeV, we observe a slight increase of the forward voltage on the three tested diodes, in the range of 2%. We observe a slight increase of the barrier height due to the Schottky interface modification, as evidenced in previously reported experiments using more damaging ion for irradiation [17]. It seems that the interface is more affected when the proton energy is low. The proton ionizing power is higher at a low energy than at a high energy which could explain partially this behavior, but this should be checked by a dedicated study. In the reverse mode, we can observe either no significant change or a slight decrease of the leakage current after the stress. We can notice that the higher the initial leakage current, the higher the decrease of the leakage current (in percentage). This reduction of the leakage current has been also observed in the first steps of the endurance and temperature step stress and disappears after a preconditioning phase of 96 h of electrothermal stress. It is important to note that the diode was dc reverse biased at 200 V during the irradiation. Neither single-event effects nor catastrophic failure has been observed for these energies and fluences. A test under dynamic switching would be requested to complete this paper. However, we can already conclude that the diodes present a high level of radiation hardness.

### Table IV

<table>
<thead>
<tr>
<th>Diode n°</th>
<th>Proton energy</th>
<th>Forward mode</th>
<th>Reverse mode</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Forward voltage @ 3 A (V)</td>
<td>Reverse current @ 300V (A)</td>
</tr>
<tr>
<td></td>
<td>Before test</td>
<td>After test</td>
<td>Before test</td>
</tr>
<tr>
<td>D30</td>
<td>100MeV</td>
<td>1.60</td>
<td>1.61</td>
</tr>
<tr>
<td>D33</td>
<td>1.92</td>
<td>1.95</td>
<td>2.58E-8</td>
</tr>
<tr>
<td>D41</td>
<td>1.75</td>
<td>1.77</td>
<td>2.55E-8</td>
</tr>
<tr>
<td>D65</td>
<td>60MeV</td>
<td>1.57</td>
<td>1.58</td>
</tr>
<tr>
<td>D66</td>
<td>1.61</td>
<td>1.62</td>
<td>1.41E-8</td>
</tr>
<tr>
<td>D99</td>
<td>1.56</td>
<td>1.54</td>
<td>1.21E-6</td>
</tr>
<tr>
<td>D100</td>
<td>15MeV</td>
<td>1.68</td>
<td>1.71</td>
</tr>
<tr>
<td>D102</td>
<td>1.66</td>
<td>1.69</td>
<td>3.32E-7</td>
</tr>
<tr>
<td>D106</td>
<td>1.67</td>
<td>1.70</td>
<td>1.86E-6</td>
</tr>
</tbody>
</table>

In this paper, 300-V 5-A Schottky diodes have been designed and fabricated for operating in solar panel arrays of the BepiColombo space mission. The package and semiconductor technologies have been made compatible to reach an operating temperature ranging from $-170 \degree C$ to $270 \degree C$. Tungsten Schottky contacts have shown to be highly stable after the long time stress at a high temperature. The main challenges were the interconnection and packaging schemes. This was solved using gold wire bonding and electroplating gold top anode metallization instead of sputtered aluminum as the high current anode metallization. On the cathode contact, the Ti/Ni/Au metallization and AuGe die-attach combination showed a very good behavior. The packaged diodes (metallic TO-257 case with an intermediate BeO isolation layer) exhibited a high stability up to working (case) temperature of $330 \degree C$. The diodes are also able to support thermal cycling from $-170 \degree C$ to $270 \degree C$. Finally, the diodes have presented a good resistance to radiation test, even if some dynamic effects on the reverse leakage current are seen in the total dose radiation test. These effects are due to the interface charges and are reversible. From the results presented here, one can conclude that the fabricated W-Au SiC diodes are suitable for the extreme working conditions required by the specific BepiColombo mission to Mercury. These devices are produced in a standard production line which includes two specific equipment: an aluminum implanter and a high-temperature ($1600 \degree C$) furnace. For this application, only small series of parts are needed, in the range of 2000. The quality control of the parts is done through a screening procedure done on each part which includes conditioning step, measurements at low and high temperatures, temperature cycling, HTRB test, power cycling, and leak tests. For a further higher volume production of these devices, a cost reduction should be envisaged through decreasing the production costs and diminishing the electrical testing.

**ACKNOWLEDGMENT**

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